Slew rate control strategies for smart power ICs based on iterative learning control

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Slew Rate Control Strategies for Smart Power ICs based on Iterative Learning Control

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***Abstract*— Smart Power ICs are Power Switches with integrated control and protection functions for the switching of middle and high current loads in industrial and automotive applications. Due to customer specifications and electromagnetic compatibility requirements it is often desired to limit the current and voltage slew rate at the output terminal of the Smart Power IC by minimizing the switching losses at the same time. In order to reduce the development effort and costs, a reusable control strategy is strived for. Therefore, a power optimal digital slew rate control strategy is developed which allows for a systematic limitation of the current and/or voltage slew rates. The strategy is based on the optimization of a gate current profile using Iterative Learning Control. A rapid prototyping test bench is developed for the verification of the control strategy. The performance and robustness is demonstrated by means of measurement results.**

I. Introduction

Power Switches with integrated control and protection functions, also known as Smart Power ICs, are widely used in industrial and automotive applications, see, e.g., [1], [2]. In order to meet the demands regarding electromagnetic compatibility, the slew rate of the current and voltage waveform at the output terminal of the Power Switch is often constrained. However, it has to be taken into account that the total power dissipation during the switching strongly depends on the slew rates. Therefore, it is necessary not only to limit but also to control the slew rate, in order to achieve maximum switching speed and power optimality. In this context, several analog control strategies have been proposed in the last decades, including feedforward [3], adaptive feedforward [4]–[6] and closed-loop [7]–[10] control strategies. However, using analog control strategies and analog circuit design necessitates major redesign effort every time the load conditions or slew rate constrains change. Obviously, this results in high costs.

The advent of cheap and powerful System-on-a-Chip solutions allows to overcome these drawbacks by a digital implementation of the control strategy. In the last years, a few digital slew rate control strategies for Power Switches have been developed and presented, see, e.g., [11]–[14]. Most of these strategies are based on adaptive feedforward control using gate current profiles or digital switchable gate resistors. In [12], for instance, an adaptive gate current profile is used to control the switching operation. The profile is divided into eight time intervals, which correspond to the operating points of the Power Switch. A constant gate current value is assigned to each interval and the length of the time intervals are iteratively adapted to compensate for model uncertainties, load variations and temperature dependencies. In [14], in addition to the length of the time interval also the amplitude of the corresponding gate current is adapted. Using an IGBT, it is shown that the slew rate can be specifically controlled by means of this approach. However, maximum switching speed and power optimality can hardly be achieved by a division of the gate current profile into only eight time intervals since the behavior of the Power Switch is highly nonlinear.

In this paper, a reusable power optimal digital control strategy is presented that is able to keep the slew rates of the terminal current and/or voltage within given bounds. For this, a highly resolved gate current profile is used as feedforward control. Model uncertainties, load and temperature variations are compensated by means of an Iterative Learning Control strategy. A rapid prototyping test bench for the verification of the developed control strategy is presented and the performance and robustness is demonstrated by means of measurement results.

II. Control Strategy

Fig. 1 depicts the block diagram of the digitally controlled Smart Power IC. Basically it consists of the digital control unit and the plant. The digital control unit may be an FPGA or a μC. The plant itself is composed of the Power Switch T_1, the gate driver, the switching load and the power supply V_{bat}. The Power Switch is operated in PWM-mode with the modulation time T_{PWM} and the duty cycle χ and is controlled by the gate current i_G generated by the gate driver.

In the following, only the control strategy for the switch-on operation is discussed for the sake of brevity. Clearly, the presented strategy is directly applicable to the switch-off operation.

During the switching time T_{on}, the switching operation is controlled by a highly resolved gate current profile $u_j[k] = u_j(kT_s), k = 0, 1, \ldots, (N-1)$, with the iteration index $j = 1, 2, \ldots$. The profile is sampled with the sampling time T_s and consists of $N = T_{\text{on}}/T_s$ samples, which

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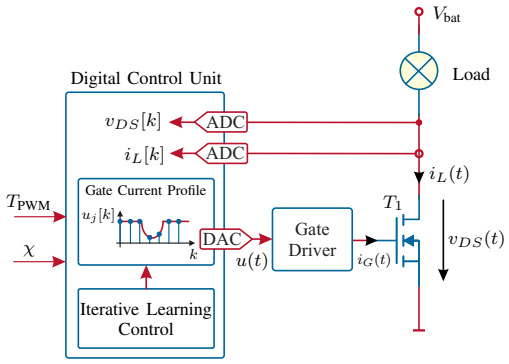

Fig. 1. Block diagram of the digitally controlled Smart Power IC.

are stored in a buffer. The profile is supplied to the gate driver using a digital-to-analog converter (DAC) in the form $u(t) = u_j(kT_s)$. The load current $i_L(t)$ and the drain-source voltage $v_{DS}(t)$ are measured and sampled by means of digital-to-analog converters (ADCs) providing $i_L[k]$ and $v_{DS}[k]$, which are also stored in a buffer.
An initial gate current profile is precalculated, e.g. by solving an optimal control problem, see [15], which is tailored to the demanded maximum slew rate and minimal switching losses. To compensate for model uncertainties, load variations and temperature dependencies, the precalculated profile has to be adapted under real operating conditions. Therefore, an Iterative Learning Control Strategy (ILC) is applied. This strategy is rewarding for systems which execute the same task multiple times, see, e.g., [16]–[18]. In this case, the performance of the system can be improved by learning from previous switching operations.

In the following, an Iterative Learning Control strategy that controls either the slew rate of the load current or the drain-source voltage is presented. Furthermore, this strategy is extended to the simultaneous control of both slew rates.

A. Control of the current or voltage slew rate

Since the current and voltage slew rate control algorithms are, from an algorithmic point of view, identical, only the voltage slew rate control concept is outlined here.
The voltage slew rate is controlled by the following ILC law

$$\bar{u}_{j+1}[k] = Q_v(\delta)\Big(u_j[k] + \gamma_v e_{v,j}[k]\Big), \tag{1a}$$

$$u_{j+1}[k] = \mathrm{sat}\Big(\bar{u}_{j+1}[k], u_{\max}, u_{\min}\Big). \tag{1b}$$

Herein $e_{v,j}[k]$ denotes the difference between the desired (maximum) slew rate v_{DSp_d} and the actual slew rate $v_{DSp,j}[k], k = 0, 1, \ldots, (N-1)$ in the iteration step j, i.e.

$$e_{v,j}[k] = v_{DSp_d} - v_{DSp,j}[k]. \tag{1c}$$

Moreover, γ_v is a constant learning gain, $Q_v(\delta)$ represents the so-called Q-filter and $\mathrm{sat}(\cdot)$ is a saturation function.

The actual slew rate is obtained by numerical differentiation of $v_{DS}[k]$. As $v_{DS}[k]$ is stored in a buffer, a non-causal filter can be utilized, e.g. a Savitzky-Golay filter, see, e.g., [19], [20]. The Savitzky-Golay filter interpolates a set of input samples by a polynomial using a least-squares approach. On the basis of the polynomial coefficients, the derivative can be calculated. The least-squares character of this approach also ensures that measurement noise does only marginally impair the results, whereas waveform height and shape are maintained. For the interpolation of $N_d = 2M + 1$ drain-source voltage samples, the polynomial of order d

$$p[m] = \sum_{i=0}^{d} c_i[k] m^i, \tag{1d}$$

with the coefficients $c_i[k], i = 0, 1, \ldots, d$, is used. The coefficients are determined in the least-squares sense by solving the minimization problem

$$\min_{c_0[k], c_1[k], \ldots, c_d[k]} \sum_{m=-M}^{M} \left(v_{DS}[k+m] - p[m]\right)^2. \tag{1e}$$

Differentiating and evaluating (1d) at $m = 0$ results in the approximated slew rate

$$v_{DSp,j}[k] = c_1[k]. \tag{1f}$$

Since $c_1[k]$ depends linearly on the measurement samples $v_{DS}[k+m]$, it can be shown, see, e.g., [20], that (1f) equals a discrete convolution of the form

$$v_{DSp,j}[k] = \sum_{m=-M}^{M} g_d[m] v_{DS}[k+m], \tag{1g}$$

with the fixed impulse response $g_d[m]$. Note, a zero-padding strategy is applied for the sample indices $k + m < 0$ and $k + m > N - 1$.

For the ILC strategy to be robust against noise and attenuate non-repetitive disturbances, the adapted profile $u_j[k] + \gamma_v e_{v,j}[k]$ is filtered with the Q-filter $Q_v(\delta)$, see, e.g., [18]. Here, δ denotes the forward time shift operator, i.e. $\delta q[k] \equiv q[k+1]$. As $v_{DSp,j}[k]$ is stored in a buffer, a zero-phase non-causal moving average filter of length N_q with Gaussian kernel [21]

$$Q(\delta) = \sum_{m=-\frac{N_q+1}{2}}^{\frac{N_q+1}{2}} \frac{T_s}{\sqrt{2\pi}\sigma_v} \exp\left(-\frac{1}{2}\left(\frac{mT_s}{\sigma_v}\right)^2\right) \delta^{-m} \tag{1h}$$

can be employed. The parameter σ_v is related to the 3-dB filter bandwidth f_c in the form

$$\sigma_v = \frac{\sqrt{\ln 2}}{2\pi f_c}. \tag{1i}$$

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The saturation function

$$u_{j+1}[k] = \mathrm{sat}\Big(\bar{u}_{j+1}[k], u_{\max}, u_{\min}\Big) = \begin{cases} u_{\max}, & \bar{u}_{j+1}[k] > u_{\max} \\ \bar{u}_{j+1}[k], & u_{\min} \le \bar{u}_{j+1}[k] \le u_{\max} \\ u_{\min}, & \bar{u}_{j+1}[k] < u_{\min} \end{cases}, \tag{1j}$$

is used as an anti-windup strategy to take into account the physical limitation of the gate driver and consequently of the gate current i_G. Here, $u_{\max}$ and $u_{\min}$ denote the upper and lower limits of the gate current profile. The presented ILC

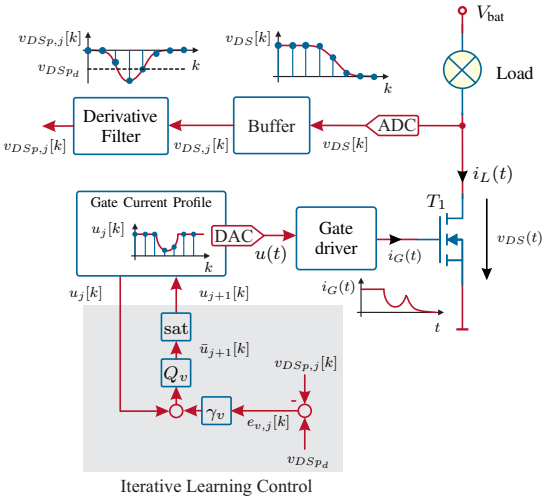

Fig. 2. ILC strategy to control the slew rate of the drain-source voltage.

strategy is summarized in Fig. 2. The convergence speed and the robustness can be adjusted by means of the learning gain γ_v and the 3-dB bandwidth f_c of the Q-filter. A high γ_v will increase the convergence speed but decrease the robustness. A high f_c tends to reduce the convergence error but also weakens the robustness, see, e.g., [22].

With the presented control strategy, the slew rate of either the load current or drain-source voltage at the output terminal of the Power Switch can be controlled to its desired (maximum) value. Thus, maximum switching speed is achieved and the occurring switching losses are minimized.

B. Simultaneous control of the current and voltage slew rate

The control strategy for the simultaneous control of the current and voltage slew rate is depicted in Fig. 3. In this case, the gate current profile $u_j[k]$ is the sum of the profiles $u_{i,j}[k]$, $u_{v,j}[k]$ and the maximum value of the gate current profile $u_{\max}$. This sum is filtered with the Q-filter $Q(\delta)$, resulting in

$$\bar{u}_{j+1}[k] = Q(\delta)\left(u_{\max} + u_{i,j+1}[k] + u_{v,j+1}[k]\right), \tag{2a}$$

and constrained using the saturation function (1j),

$$u_{j+1}[k] = \mathrm{sat}\Big(\bar{u}_{j+1}[k], u_{\max}, u_{\min}\Big), \tag{2b}$$

in order to the limit the gate current profile to its maximal and minimal value $u_{\max}$ and $u_{\min}$.

Maximum switching speed would be achieved if $u_{\max}$ would be applied for the whole switching operation. However, the gate current profile has to be changed by $u_{i,j}[k]$ and $u_{v,j}[k]$ in order to avoid that the current and voltage slew rates $i_{Lp,j}[k]$ and $v_{DSp,j}[k]$ exceed their bounds i_{Lp_d} and v_{DSp_d}, respectively.

To compensate for plant uncertainties, these profiles are iteratively adapted using the ILC laws

$$\bar{u}_{i,j+1}[k] = Q_i(\delta)\left(u_{i,j}[k] + \gamma_i e_{i,j}[k]\right), \tag{2c}$$

$$u_{i,j+1}[k] = \mathrm{sat}\Big(\bar{u}_{i,j+1}[k], 0, -u_{\max}\Big) \tag{2d}$$

and

$$\bar{u}_{v,j+1}[k] = Q_v(\delta)\left(u_{v,j}[k] + \gamma_v e_{v,j}[k]\right), \tag{2e}$$

$$u_{v,j+1}[k] = \mathrm{sat}\Big(\bar{u}_{v,j+1}[k], 0, -u_{\max}\Big) \tag{2f}$$

with the learning gains γ_i and γ_v, the Q-filters $Q_i(\delta)$ and $Q_v(\delta)$ and the differences between the desired (maximum) slew rates and the actual slew rates of the load current and the drain-source voltage

$$e_{i,j}[k] = i_{Lp_d} - i_{Lp,j}[k] \tag{2g}$$

and

$$e_{v,j}[k] = v_{DSp_d} - v_{DSp,j}[k]. \tag{2h}$$

Using the presented strategy, the current and voltage slew rates can be kept below their desired maximum values. Since $u_{\max}$ serves as a non adaptive feedforward term, maximum switching speed and therefore minimal switching losses are achieved.

III. Rapid Prototyping Test Bench

Fig. 4 shows the block diagram of the rapid prototyping test bench. The test bench consists of the dSPACE real-

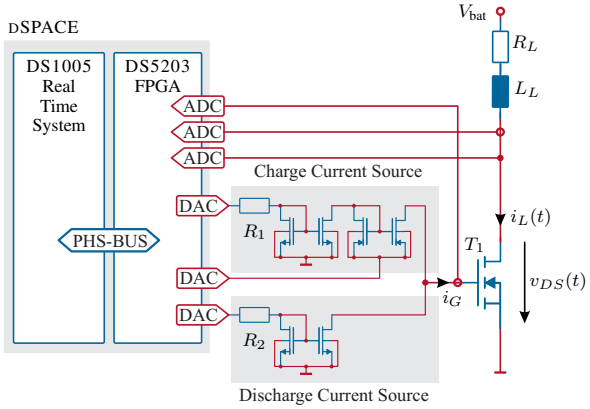

Fig. 4. Block diagram of the rapid prototyping test bench.

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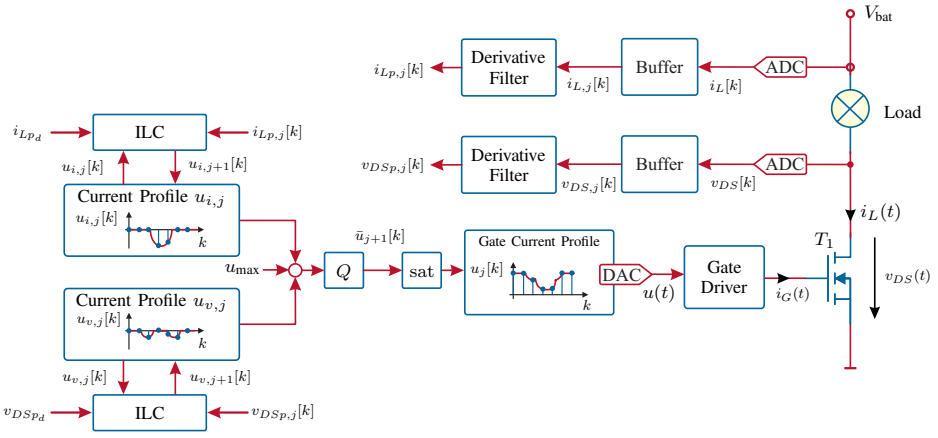

Fig. 3. ILC strategy for the simultaneous control of the current and voltage slew rate.

time measurement and control system DS1005 PPC with the DS5203 FPGA extension board, the controllable charge and discharge current source, the Power Switch T_1, the battery voltage V_{bat} and the ohmic/inductive switching load R_L and L_L. The dSPACE system allows for the rapid code generation and programming with MATLAB/SIMULINK and the FPGA code generation was performed with the XILINX SYSTEM GENERATOR FOR DSP. The dSPACE CONTROLDESK software is used for control and signal processing of the test bench. The drain-source voltage $v_{DS}(t)$ is measured directly, for the load current $i_L(t)$ the magnetoresistive current sensor CMS3005 from SENSITEC is employed, and the gate current $i_G(t)$ is measured with a shunt and the preamplifier SR560 from STANFORT RESEARCH SYSTEMS. All measurements are sampled with 14 bit by means of the 10 MSPS ADCs of the FPGA board. The input range of the ADC is $\pm 5\,\text{V}$ for i_G and i_L and $\pm 30\,\text{V}$ for v_{DS}. Moreover, the charge and discharge current sources of the gate driver are controlled by the 14 bit, 10 MSPS DACs of the FPGA board. The DACs exhibit a maximum output voltage of $\pm 10\,\text{V}$. The current sources provide a controllable gate-current approximately between $\pm 0.8\,\text{mA}$. A photo of the rapid prototyping test bench is shown in Fig. 5.

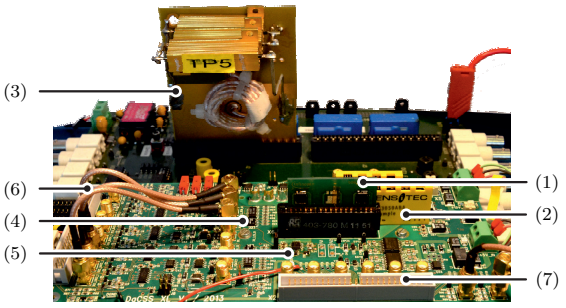

Fig. 5. Rapid prototyping test bench: (1) Power Switch; (2) current sensor; (3) ohmic/inductive load; (4) charge current source; (5) discharge current source; (6) and (7) interface to the dSPACE system.

IV. IMPLEMENTATION AND MEASUREMENT RESULTS

For the following experiments, the Power MOSFET BSC020N03 was chosen to switch an ohmic/inductive load of $R_L = 3.2\,\Omega$, $L_L = 14\,\mu\text{H}$ at a battery voltage of $V_{\text{bat}} = 13.5\,\text{V}$. The PWM time was set to $T_{\text{PWM}} = 10\,\text{ms}$ with a duty cycle of $\chi = 0.5$. Using the FPGA and its ADCs, the switching waveforms of i_L and v_{DS} are sampled with $T_s = 0.1\,\mu\text{s}$ and written into buffers of $N = 1000$ samples each. The ILC algorithm itself is executed every 20 ms on the real-time system DS1005. Therefore, the gate current profiles are adapted after every second switching operation. After the adaptation of the gate current profiles for the switch-on and switch-off operation, they are transmitted to the FPGA and applied to the gate driver using the DACs. For the estimation of $i_{Lp,j}[k]$ and $v_{DSp,j}[k]$, the length of the Savitzky-Golay filter, see (1g), was chosen as $N_d = 21$ and a second order polynomial, $d = 2$, was used. This results in the coefficients $g_d[m] = -m/(280T_s)$. The length of the Q-filters Q_v, Q_i and Q, see (1h), was set to $N_q = 17$ and the 3-dB frequency was experimentally chosen as $f_c = 1.32\,\text{MHz}$. The limits of the gate current profile, see (1j), were set to $u_{\text{max}} = 8000$ and $u_{\text{min}} = 652$ for the switch-on operation and $u_{\text{max}} = 8000$ and $u_{\text{min}} = 300$ for the switch-off operation.

The measurement results for the slew rate control of the load current are presented in Fig. 6, for the drain-source voltage in Fig. 7 and for the simultaneous control in Fig. 8. Fig. 9 depicts the gate current profiles corresponding to Fig. 8. On the left-hand side of each figure, the switch-on operation and on the right-hand side, the switch-off operation is presented. The different gate current profiles can be found in the first row and the resulting gate current i_G is shown in the second row. The drain-source voltage v_{DS} and its derivative $\text{d}v_{DS}/\text{d}t$ are given in the third and fourth row, respectively. The last two rows illustrate the time evolution of the load current and its derivative.

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The switching of an inductive load results in high drain-source voltage transients at the end of the switch-off operation, cf. Fig. 6-8. With the presented strategy, the slew rate of these transients is not directly controllable. However, their shape and amplitude can be influenced by controlling the slew rate during the switch-off operation.

It is evident that by means of the presented control strategies the desired maximal slew rates are met. It is worth noting that the control strategies also pursue the goal to minimize the switching losses. This is why, the time evolutions of the load current and the drain-source voltage reach their respective desired maximum slew rates for a quite long time during the switch-on and switch-off phase, which can be seen in Fig. 6-8.

V. Conclusion

In this paper, a digital control strategy was presented that limits the current and/or voltage slew rate at the output terminal of a Smart Power IC within given bounds and guarantees power optimality at the same time. The digital control strategy is based on an adaptive feedforward control strategy using a highly resolving gate current profile. In order to be able to handle model uncertainties due to fabrication tolerances, load variations and temperature dependencies, the gate current profile is adapted by means of an Iterative Learning Control strategy. A rapid prototyping test bench was presented and the performance and robustness of the proposed approach was demonstrated by means of measurement results. Future work will be concerned with the hardware and performance requirements for series production as well as the improvement of the adaptation speed for a rapid load change.

Acknowledgment

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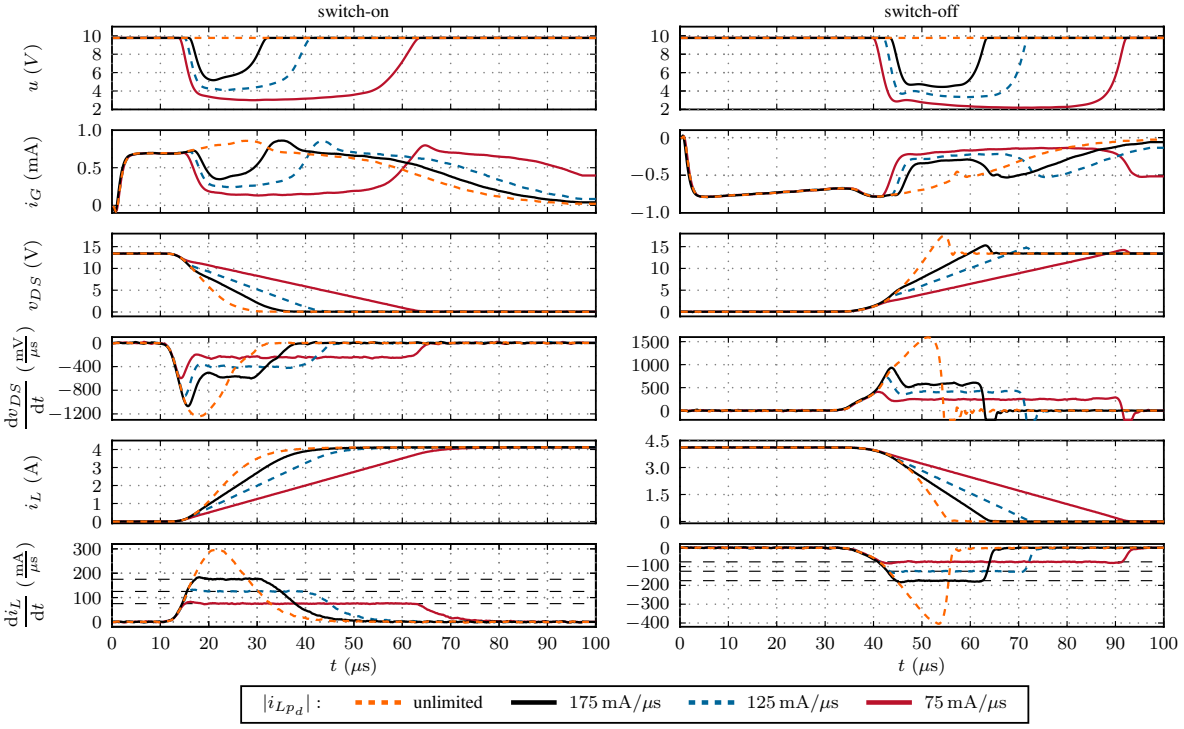

Fig. 6. Measurement results of the load current slew rate control with $\gamma_i^{\mathrm{on}} = -\gamma_i^{\mathrm{off}} = 0.5\,\mu\mathrm{s/mA}$, $R_L = 3.2\,\Omega$, $L_L = 14\,\mu\mathrm{H}$ and $V_{\mathrm{bat}} = 13.5\,\mathrm{V}$.

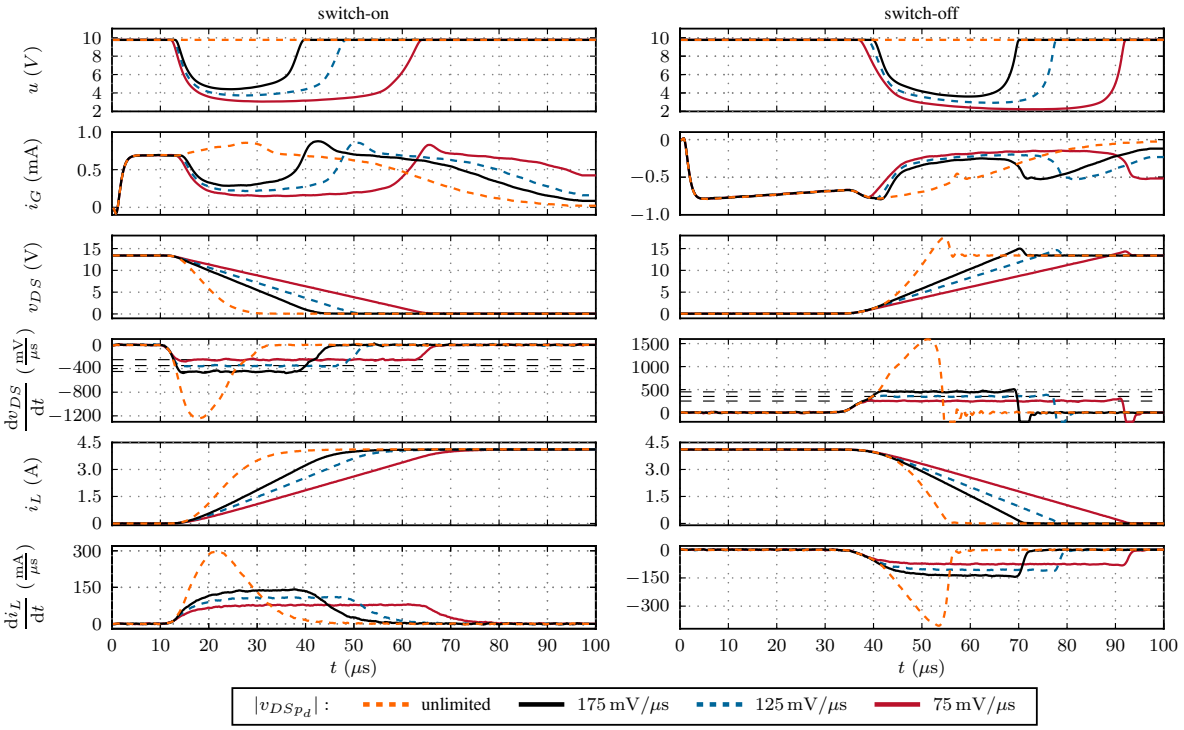

Fig. 7. Measurement results of the drain-source voltage slew rate control with $\gamma_v^{\mathrm{on}} = -\gamma_v^{\mathrm{off}} = -0.1\,\mu\mathrm{s/mV}$, $R_L = 3.2\,\Omega$, $L_L = 14\,\mu\mathrm{H}$ and $V_{\mathrm{bat}} = 13.5\,\mathrm{V}$.

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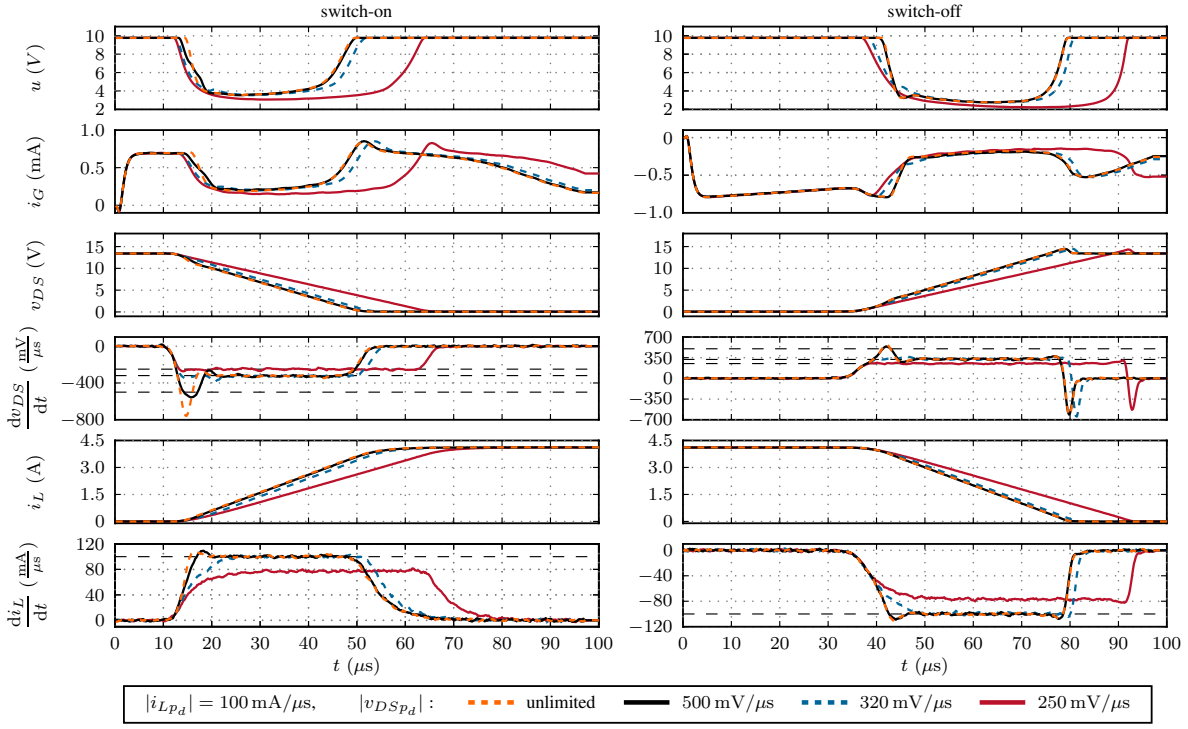

Fig. 8. Measurement results of the simultaneous load current and drain-source voltage slew rate control with $\gamma_i^{\mathrm{on}} = -\gamma_i^{\mathrm{off}} = 0.5\,\mu\mathrm{s/mA}$, $\gamma_v^{\mathrm{on}} = -\gamma_v^{\mathrm{off}} = -0.1\,\mu\mathrm{s/mV}$, $R_L = 3.2\,\Omega$, $L_L = 14\,\mu\mathrm{H}$ and $V_{\mathrm{bat}} = 13.5\,\mathrm{V}$.

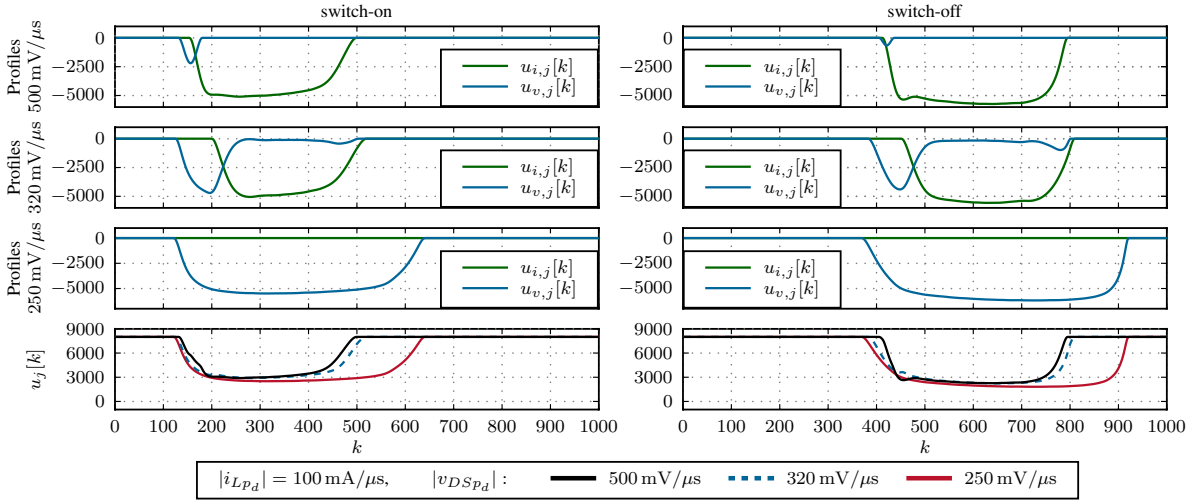

Fig. 9. Gate current profiles corresponding to Fig. 8 for the switch-on and switch-off operation using $\gamma_i^{\mathrm{on}} = -\gamma_i^{\mathrm{off}} = 0.5\,\mu\mathrm{s/mA}$, $\gamma_v^{\mathrm{on}} = -\gamma_v^{\mathrm{off}} = -0.1\,\mu\mathrm{s/mV}$, $R_L = 3.2\,\Omega$, $L_L = 14\,\mu\mathrm{H}$ and $V_{\mathrm{bat}} = 13.5\,\mathrm{V}$.

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