Digital slew rate and S-shape control for Smart Power Switches to reduce EMI generation

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***Abstract*—Smart Power Switches are power switches with integrated control and protection functions for the switching of middle and high current loads. In particular in automotive applications, Smart Power Switches have to be operated without additional stabilization networks, EMI filters, and heat sinks to keep the weight, required space and costs of the circuit boards as low as possible. Therefore, the generated electromagnetic emissions must be reduced by another measure without significantly increasing the switching losses. This can be achieved by the active control of the first and/or second derivative of the output voltage. This paper presents a digital slew rate control and its extension to an S-shape control strategy which, in addition to the slew rate, also controls the second derivative of the output voltage. Both strategies are based on feedforward gate current profiles which are iteratively adapted by an Iterative Learning Control strategy to compensate for load variations and temperature dependencies. A rapid prototyping test bench is presented, and the performance and robustness of the control strategies are demonstrated by a series of measurement results. An EMC compliance test according to the CSIPR 25 standard shows that the generation of conducted electromagnetic emissions can be reduced in a power efficient way by the proposed approach.**

I. Introduction

Smart Power Switches are power switches with integrated control and protection functions for the switching of current loads of about 0.5 to 40 A. They are widely used in automotive and industrial applications where they operate at a switching frequency from 100 up to 1000 Hz with a turn-on and turn-off time from 20 to 200 μs [1]–[3]. Fig. 1 shows some typical automotive applications for a Smart Power Switch which are, e.g., the switching of heating elements like seat heating and glow plug, control of DC brush motors for pumps and fans as well as the switching of exterior and interior lighting bulbs [4]. Rapid switching of high current loads typically provokes the unintentional generation of electromagnetic interferences (EMI). These conducted and radiated emissions interfere with other electronic circuits and have to be limited in order to meet the standards on electromagnetic compatibility (EMC). In the considered case of Smart Power Switches, the switching operation mainly generates conducted broadband disturbances up to 2 MHz. A common method to reduce these conducted EMI is the application of EMI-filters [5]. These mostly bulky filters are undesirable, mainly because of the following reasons. First, they cannot be integrated on the chip due to their size and secondly, additional components on the circuit boards, like stabilization networks or heat sinks, cause additional costs, weight and space requirements.

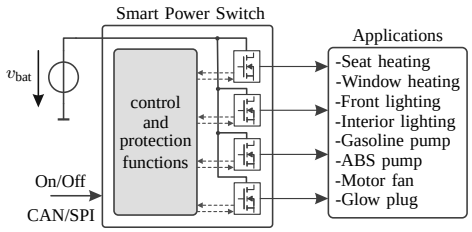

Fig. 1. Smart Power Switch and its applications.

Consequently, the generation of EMI has to be suppressed at its source, the switching operation: This can be achieved by the control and limitation of the first and higher derivatives of the switching transition. Higher order derivative control was first shown in [5] to reduce spectral power in switching nodes. In particular the rectangular limitation of the second derivative has been proven in theory in [6] to improve the achievable trade-off between switching losses and EMI reduction. The resulting switching transition is S-shaped. Other appropriate transitions to reduce EMI are, e.g., of sinusoidal shape [7]–[9] or of Gaussian-shape [10], [11]. In [5], [7], [8], [10], [11], analog closed-loop trajectory tracking strategies are applied. The trajectory tracking control strategy minimizes the error between the actual switching transition and the precalculated desired switching trajectory, i.e., a sinusoidal or Gaussian shape trajectory. However, the calculation of a desired switching trajectory demands specific information about the switching characteristics of the power switch and the switching load, i.e., the battery voltage and the load condition. Whereas the switching characteristics of the power switch can be assumed to be known, the battery voltage and the load condition can vary with time and the desired switching trajectory has to be adapted to the changed conditions. In contrast to tracking strategies, derivative control strategies only limit the first and higher derivatives of the

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switching transitions and thus are able to reduce the EMI independent of the system voltage, load condition, and the characteristics of the power switch. Therefore, this work is concerned with the control of the first and second derivatives of the switching transitions.

Until now, the switching transition in Smart Power Switches are controlled by analog control circuits which control the first derivative, resp. the slew rate, of the output voltage [3]. In literature, analog slew rate control strategies can mainly be found for fast switching IGBTs, e.g., [12]–[14]. However, analog control strategies are designed for a certain power switch, load condition and slew rate and are hardly reusable for other power switches and applications without a major redesign of the analog control circuit. Clearly, this results in higher development efforts and thus in higher costs, in particular for the development of integrated circuits.

The advent of cheap and powerful System-on-a-Chip (SoC) solutions allows these drawbacks to be overcome by a digital implementation of the control strategy. Apart from the fact that a digital control concept can be easily adapted to different circuit designs and power classes it also enables the application of more advanced control strategies such as nonlinear and adaptive control.

In [15], so-called feedforward gate current profiles are used to control the slew rate of the output voltage of an IGBT. In [16], the gate current profile was tuned to also control higher order derivatives of the switching transition to improve the trade-off between EMI reduction and switching losses. The profiles are generated by a waveform generator and applied to the IGBT by a controllable gate drive without considering any feedback information. It is clear that such pure feedforward gate current profiles cannot cope with changing circuit conditions and therefore are not viable for real systems.

Recently, a few adaptive feedforward slew rate control strategies for IGBTs have been presented in [17], [18], and [19]. In these works, the gate current profiles are iteratively adapted from switching cycle to switching cycle to account for dead times and to compensate model uncertainties, temperature dependencies, and load variations. In [18], for instance, the profile is divided into eight time intervals corresponding to the operating points of the IGBT. A constant gate current value is assigned to each interval and the lengths of the time intervals are iteratively adapted. In [19], additionally to the adaption of the time interval length, also the amplitude of the corresponding gate current is modified. Using an IGBT, it is shown that the slew rate in fact can be specifically controlled by this approach. However, since the behavior of the IGBT is highly nonlinear, the segmentation of the gate current profile into eight time intervals might not be sufficient to ideally control the slew rate to its desired limits, which may result in increased switching losses or reduced EMC performance.

The limitation of the slew rate inevitably slows down the switching speed and therefore increases the switching losses, which in turn generates additional heat losses. These additional thermal losses are problematic for the operation of Smart Power Switches because they have to be operated without additional heat sinks or other cooling methods on the circuit board [1]. Therefore, it is of vital importance not only to limit the slew rate to its desired value but, at the same time, to keep the switching losses to a minimum. Furthermore, the control and limitation of higher derivatives has to be considered to improve the tradeoff between EMI reduction and switching losses.

In contrast to IGBTs, the turn-on and turn-off times of the considered Smart Power Switches are significantly longer. For switching times in the range of 20 to 200 μs, modern low cost SoC technology allows to process highly resolved gate current profiles, to sample the switching transients at a high frequency, and to calculate the first and second derivative from the sampled data. Therefore, this paper presents a slew rate control strategy which relies on highly resolved gate current profiles. Furthermore, the slew rate control strategy is extended to also control the second derivative of the switching transient so that an S-shape waveform can be realized on low cost hardware.

The paper is organized as follows: Section II introduces the slew rate control strategy that iteratively adapts the gate current profile by an Iterative Learning Control (ILC) strategy [20]–[22] to compensate model uncertainties, and load and temperature variations. Afterwards, the slew rate control is extended to an S-shape control concept. Both strategies are implemented on a rapid prototyping test bench which is presented in Section III. Section IV is concerned with the implementation of the two strategies whose performance and robustness are demonstrated by measurement results. The impact of the control strategies on the conducted EMI is investigated by an EMC compliance test according to the CSIPR 25 standard [23]. The last section, Section V, summarizes the results.

The results show that the presented slew rate control strategy is not only able to limit the slew rate but to ideally control it to its desired bound. Furthermore, the measurement results confirm that in particular the control of the second derivative constitutes a good trade-off between EMI reduction and switching losses. Moreover, the control concept can cope with changing load conditions, is independent of device and package choice, and is robust against switching and measurement noise.

II. Control Strategy

The switch-on and switch-off operation is separately controlled by the proposed control strategy. For the sake of brevity, only the switch-on operation will be considered in the following. However, all the concepts are directly applicable to the switch-off operation. If there are any differences they will be stated explicitly.

In [24] it was shown that by the control of the load current slew rate the first derivative of the output voltage exhibits a spike at the beginning of the switching transition. This spike may cause an increase of the EMI level instead of a reduction. Therefore, only voltage control strategies are

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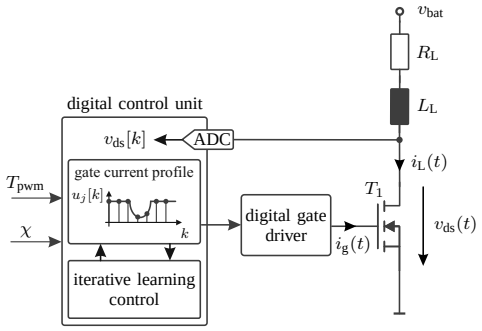

Fig. 2. Digitally controlled Smart Power Switch including switching load.

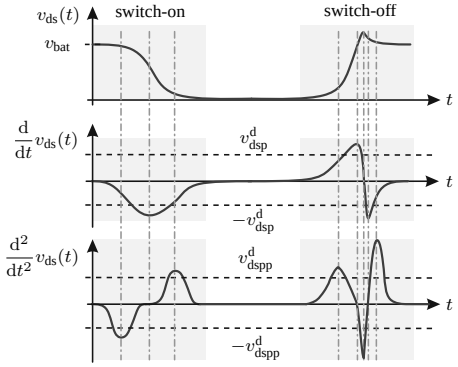

Fig. 3. Sketch of the switching transition of $v_{\text{ds}}(t)$ and its first and second derivatives.

considered in the following. However, the control strategies are also directly applicable to the load current. Before the control law is outlined in detail, the uncontrolled switching behavior of the power switch is discussed and the control objectives are formulated.

A. Control Objectives

Fig. 2 depicts a schematic diagram of a digitally controlled Smart Power Switch including the ohmic/inductive switching load R_{L} and L_{L} and the battery voltage v_{bat}. The power MOSFET T_1 switches the load with the time period T_{pwm} and the duty cycle χ. The switching operation of T_1 is controlled by the highly resolved gate current profile $u_j[k] = u_j(kT_{\text{s}})$ where j denotes the iteration index and $k = 0, \ldots, N-1$ the sampling index. The profile is sampled with the sampling time T_{s} and N samples are stored in a buffer of the digital control unit. The gate current profile is converted by the digitally controllable gate driver to the gate current i_{g}, which is applied to the power MOSFET. The corresponding drain-source voltage $v_{\text{ds}}(t)$ is measured and sampled, and N samples are stored in a buffer of the digital control unit, i.e., $v_{\text{ds},j}[k] = v_{\text{ds},j}((k+m)T_{\text{s}})$. Note that $v_{\text{ds},j}$ is shifted by m samples to account for system dead times, e.g., the conversion times of the ADCs and the gate driver.

The application of a constant gate current profile with $u_j[k] = u_{\text{max}}$ results in the switching transition depicted in Fig. 3. During the switching operation, the first and second derivative of the drain-source voltage, $\text{d}v_{\text{ds}}(t)/\text{d}t$ and $\text{d}^2v_{\text{ds}}(t)/\text{d}t^2$, typically exceed some desired maximum value of the first and/or second order derivatives, $|v^{\text{d}}_{\text{dsp}}|$ and $|v^{\text{d}}_{\text{dspp}}|$, respectively. Especially during the switch-off operation, $\text{d}v_{\text{ds}}(t)/\text{d}t$ and $\text{d}^2v_{\text{ds}}(t)/\text{d}t^2$, can exceed their desired maximum value multiple times because of inductive spiking. The basic idea of the control strategy is that the time transitions of $\text{d}v_{\text{ds}}(t)/\text{d}t$ and $\text{d}^2v_{\text{ds}}(t)/\text{d}t^2$ are controlled to their corresponding constraints with an optimal feedforward gate current profile $u_j[k] = u^*[k]$. The gate current profile not only ensures that the transitions stay within their constraints but even pushes them to the limits, thus resulting in maximum switching speed and therefore minimal switching losses. The optimal profile $u^*[k]$ can, e.g., be determined by solving an optimal control problem [25]. However, the calculated optimal gate current profile might still result in a violation of one of the control constraints or in reduced switching speed because of unknown load conditions as well as model uncertainties and temperature dependencies. Therefore, the gate current profile is adapted from switching cycle to switching cycle by an Iterative Learning Control (ILC) strategy. ILC is rewarding for systems that execute a task multiple times [20]–[22]. In the considered case of a Smart Power Switch, the gate current profile is adapted based on measurements of the drain-source voltage.

In the following, the slew rate control strategy and its extension to an S-shape control are explained in more detail.

B. Slew Rate Control

The slew rate is controlled by the feedforward gate current profile $u_j[k]$ which is adapted from switching cycle to switching cycle by the ILC law

$$\bar{u}_{j+1}[k] = q[k] * \Big(u_j[k] + \delta\gamma e_j[k]\Big), \tag{1a}$$

$$u_{j+1}[k] = \text{sat}\Big(\bar{u}_{j+1}[k], u_{\text{max}}, u_{\text{min}}\Big). \tag{1b}$$

Herein, $\gamma > 0$ is a constant learning gain, q represents the so-called Q-filter, $*$ is the discrete convolution operator, and $\text{sat}(\cdot)$ is a saturation function which limits the gate current profile to its maximum and minimum value u_{max} and u_{min}. The constant δ is defined as $\delta = -1$ for the switch-on operation and $\delta = 1$ for the switch-off operation. Furthermore, $e_j[k]$ denotes the difference between the slew rate constraint $v^{\text{d}}_{\text{dsp}} > 0$ and the actual slew rate $v_{\text{dsp},j}[k]$ of the current iteration j, i.e.,

$$e_j[k] = \delta v^{\text{d}}_{\text{dsp}} - v_{\text{dsp},j}[k]. \tag{2}$$

It is worth noting that the desired slew rate $v^{\text{d}}_{\text{dsp}}$ has not to be constant for the whole switching operation and different slew rates may be applied for different segments.
The Q-filter in (1a) serves as a kind of forgetting factor. It basically prevents the control law from learning non-repetitive disturbances and noise and therefore increases the robustness

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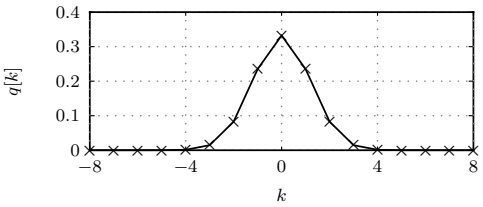

Fig. 4. Impulse response of the Q-filter with $f_c = 0.221\,\text{MHz}$, $T_s = 0.5\,\mu\text{s}$ and $N_q = 8$.

of the control strategy. In literature [26], [27], the Q-filter is often based on the Gaussian distribution

$$g(t) = \frac{1}{\sigma_q\sqrt{2\pi}} \exp\left(-\frac{t^2}{2\sigma_q^2}\right), \tag{3a}$$

with the standard deviation σ_q which is related to the 3-dB bandwidth f_c in the form

$$\sigma_q = \frac{\sqrt{\ln(2)}}{2\pi f_c}. \tag{3b}$$

To obtain the Q-filter, the Gaussian distribution (3a) is discretized

$$g[k] = \frac{1}{\sigma_q\sqrt{2\pi}} \exp\left(-\frac{k^2}{2\sigma_q^2}\right), \qquad k \in \mathbb{N}, \tag{4}$$

windowed with a rectangular window of length $2N_q + 1$ and normalized, i.e.,

$$q[k] = \frac{g[k]}{\sum_{m=-N_q}^{N_q} g[m]} \qquad \text{for} \qquad |k| \le N_q. \tag{5}$$

The window length has to be chosen sufficiently long so that the truncation error is negligible. Fig. 4 shows an example of a Q-filter with the parameters $f_c = 0.221\,\text{MHz}$, $T_s = 0.5\,\mu\text{s}$ and $N_q = 8$.

To illustrate the principle of the ILC law (1), let us assume the following scenarios for the switch-on operation: The slew rate of the switching transient violates the lower constraint for $k = k_s, \ldots, k_e$. The violation results in $e_j[k] > 0$, see (2) and Fig. 3, and therefore the gate current profile is lowered for the next switching operation, i.e., $\bar{u}_{j+1}[k] < \bar{u}_j[k]$. The reduction of the gate current profile slows down the switching speed and reduces the slew rate. If the actual slew rate is smaller than the maximum allowed value, the resulting negative error $e_j[k]$ leads to an increase of the gate current profile for the next switching operation, i.e., $\bar{u}_{j+1}[k] > \bar{u}_j[k]$. Consequently, switching speed is increased. In real operation, both scenarios described above may occur until the adapted gate current profile convergences and ideally controls the slew rate. The convergence speed and the robustness of the adaptation of the gate current profile can be adjusted by means of the learning gain γ and the 3-dB bandwidth of the Q-filter f_c. A high γ improves the convergence speed but decreases the robustness of the algorithm [26], [28]. A high f_c tends to reduce the convergence error but weakens the robustness against measurement noise and errors of the initial value [26],

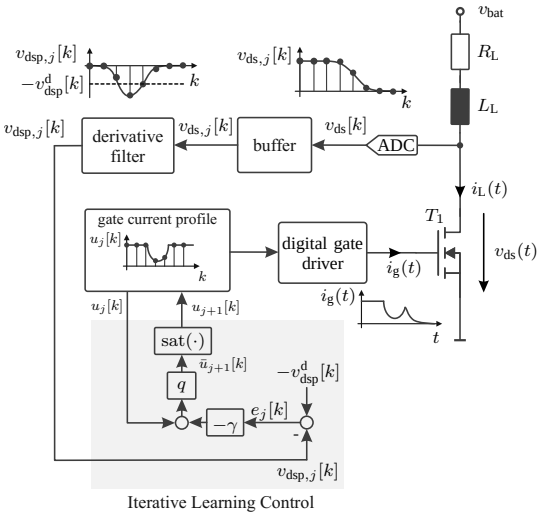

Fig. 5. Slew rate control strategy for the switch-on operation based on ILC.

[28]. The actual slew rate $v_{dsp,j}[k]$ in (2) is obtained by numerical differentiation of $v_{ds,j}[k]$. As $v_{ds,j}[k]$ is stored in a buffer, a non-causal filter can be utilized, e.g., a Savitzky-Golay filter [29], [30]. The Savitzky-Golay filter interpolates a set of input samples by a polynomial using a least-squares approach. On the basis of the polynomial coefficients, the derivative can be calculated. The least-squares character of this approach also ensures that measurement noise does only marginally impair the results and that the height and shape of the signal are maintained. For the considered case, the polynomial

$$p[m] = \sum_{i=0}^{d} c_i[k] m^i \tag{6}$$

of order d with the coefficients $c_i[k], i = 0, 1, \ldots, d$, is chosen to interpolate $2N_d + 1$ samples of $v_{ds,j}$. The coefficients of the polynomial are determined by solving the minimization problem

$$\min_{c_0[k], c_1[k], \ldots, c_d[k]} \sum_{m=-N_d}^{N_d} \left(v_{ds,j}[k+m] - p[m]\right)^2. \tag{7}$$

The differentiation and evaluation of (6) at $m = 0$ results in the approximated slew rate

$$v_{dsp} = c_1[k]. \tag{8}$$

Since $c_1[k]$ depends linearly on $v_{ds,j}[k+m]$ with $m = -N_d, \ldots, N_d$, it can be shown, see [30], that (8) equals a discrete convolution of $v_{ds,j}[k]$ with an impulse response $g_d[m]$, i.e.,

$$v_{dsp,j}[k] = \sum_{m=-N_d}^{N_d} g_d[m] v_{ds,j}[k-m]. \tag{9}$$

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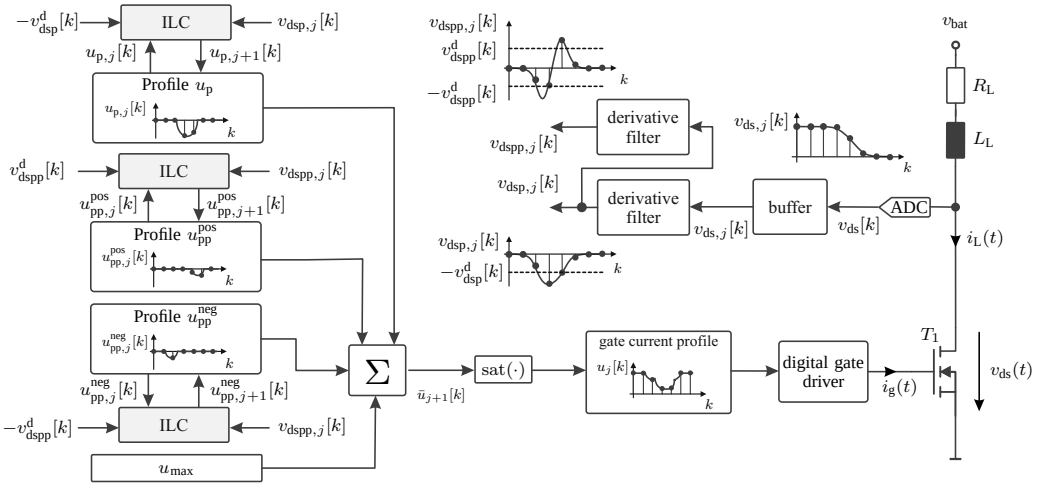

Fig. 6. S-Shape control strategy for the switch-on operation based on ILC.

For example, the Savitzky-Golay filter for $d = 2$ and $N_d = 2$ yields

$$g_\mathrm{d}[m] = -\frac{m}{10T_s}, \qquad m = -N_d, \ldots, N_d. \tag{10}$$

Note that the Q-filter and the Savitzky-Golay filter operate in different domains. While the Savitzky-Golay filter is used in the time domain to obtain suitable numerical approximations of the time derivatives of the output voltage, the Q-filter operates in the iteration domain and increases the robustness of the control strategy with respect to measurement noise. For the practical implementation of (9), a zero-padding strategy is applied to the sample indices $k - m < 0$ and $k - m > N - 1$. The overall control strategy is summarized in Fig. 5.

C. S-shape control

During the switching operation, also the second derivative may exceed its lower or its upper constraint $\pm v_\mathrm{dspp}^\mathrm{d}$, see Fig. 3. Therefore, an S-shape control strategy is designed to guarantee that the constraints in the second derivative are met in addition to the slew rate constraint. Similar to the simpler slew rate control presented in the previous subsection, the switching operation is controlled by an adaptive gate current profile $u_{j+1}[k]$. However, in the S-shape control strategy, the gate current profile consists of four additive terms

$$u_{j+1}[k] = u_\mathrm{max} + u_{\mathrm{p},j+1}[k] + u_{\mathrm{pp},j+1}^\mathrm{pos}[k] + u_{\mathrm{pp},j+1}^\mathrm{neg}[k]. \tag{11}$$

The term u_max achieves maximum switching speed whereas the violation of the constraints is accounted for by the corresponding additive profiles u_p for v_dsp, $u_\mathrm{pp}^\mathrm{pos}$ for $v_\mathrm{dspp}^\mathrm{d}$ and $u_\mathrm{pp}^\mathrm{neg}$ for $-v_\mathrm{dspp}^\mathrm{d}$. Under the assumption that the three constraints are not violated simultaneously, the additive profiles can be adapted from switching cycle to switching cycle with the three independent ILC laws

$$\bar{u}_{\mathrm{p},j+1}[k] = q_\mathrm{p}[k] * \left(u_{\mathrm{p},j}[k] + \delta\gamma_\mathrm{p} e_{\mathrm{p},j}[k]\right), \tag{12a}$$

$$\bar{u}_{\mathrm{pp},j+1}^\mathrm{pos}[k] = q_\mathrm{pp}[k] * \left(u_{\mathrm{pp},j}^\mathrm{pos}[k] + \gamma_\mathrm{pp} e_{\mathrm{pp},j}^\mathrm{pos}[k]\right), \tag{12b}$$

and

$$\bar{u}_{\mathrm{pp},j+1}^\mathrm{neg}[k] = q_\mathrm{pp}[k] * \left(u_{\mathrm{pp},j}^\mathrm{neg}[k] - \gamma_\mathrm{pp} e_{\mathrm{pp},j}^\mathrm{neg}[k]\right). \tag{12c}$$

Here, γ_p and γ_pp denote constant positive learning gains and q_p and q_pp refer to Q-filters with a Gaussian filter kernel according to (5). The control errors $e_{\mathrm{p},j}[k]$, $e_{\mathrm{pp},j}^\mathrm{pos}[k]$ and $e_{\mathrm{pp},j}^\mathrm{neg}[k]$ are given by

$$e_{\mathrm{p},j}[k] = \delta v_\mathrm{dsp}^\mathrm{d} - v_{\mathrm{dsp},j}[k], \tag{13a}$$

$$e_{\mathrm{pp},j}^\mathrm{pos}[k] = v_\mathrm{dspp}^\mathrm{d} - v_{\mathrm{dspp},j}[k], \tag{13b}$$

$$e_{\mathrm{pp},j}^\mathrm{neg}[k] = -v_\mathrm{dspp}^\mathrm{d} - v_{\mathrm{dspp},j}[k], \tag{13c}$$

whereas the second derivative $v_{\mathrm{dspp},j}[k]$ is determined by applying the derivative filter (10) to $v_{\mathrm{dsp},j}[k]$.

To achieve an admissible gate current profile, $u_\mathrm{min} \leq u_{j+1}[k] \leq u_\mathrm{max}$, the additive profiles are constraint in the form

$$u_{\mathrm{pp},j+1}^\mathrm{pos}[k] = \mathrm{sat}\left(\bar{u}_{\mathrm{pp},j+1}^\mathrm{pos}[k], 0, -u_\mathrm{max} + u_\mathrm{min}\right), \tag{14a}$$

$$u_{\mathrm{pp},j+1}^\mathrm{neg}[k] = \mathrm{sat}\left(\bar{u}_{\mathrm{pp},j+1}^\mathrm{neg}[k], 0, -u_\mathrm{max} + u_\mathrm{min}\right), \tag{14b}$$

and

$$u_{\mathrm{p},j+1}[k] = \mathrm{sat}\Big(\bar{u}_{\mathrm{p},j+1}[k], 0, -u_\mathrm{max} + u_\mathrm{min} - u_{\mathrm{pp},j+1}^\mathrm{pos}[k] - u_{\mathrm{pp},j+1}^\mathrm{neg}[k]\Big). \tag{14c}$$

Thereby, it is presumed that the constraints of the second derivative according to (12b) and (12c) are not violated at the same time. However, there may be an overlap of the profile for limiting the first derivative according to (12a) with (12b) or (12c), respectively. In this case, the addition of the profiles due to (11) will cause a violation of the constraints $u_\mathrm{min} \leq u_{j+1}[k] \leq u_\mathrm{max}$. To prevent this situation, the profile for the first derivative is limited between 0 and $-u_\mathrm{max} + u_\mathrm{min} - u_{\mathrm{pp},j+1}^\mathrm{pos}[k] - u_{\mathrm{pp},j+1}^\mathrm{neg}[k]$, see (14c), thus prioritizing the limitation of the second derivative. Fig. 6 summarizes the basic idea of the S-shape control strategy.

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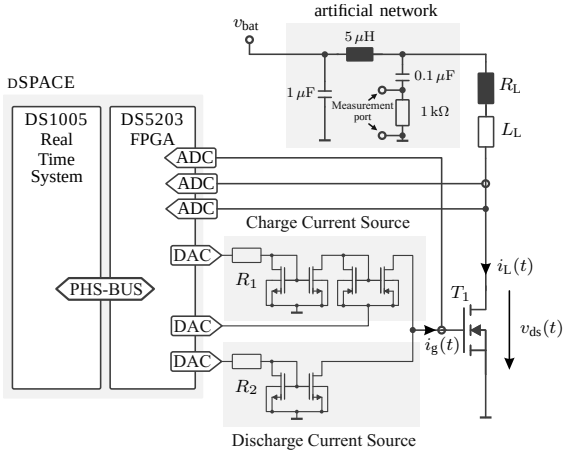

Fig. 7. Block diagram of the rapid prototyping test bench.

III. Rapid Prototyping Testbench

Fig. 7 shows the block diagram of the rapid prototyping test bench. The test bench consists of a dSPACE real-time measurement and control system DS1005 PPC with a DS5203 FPGA extension board, a controllable charge and discharge current source, the power MOSFET T_1, the battery voltage v_{bat}, and the ohmic/inductive switching load R_L and L_L. The dSPACE system allows for rapid code generation and programming with MATLAB/SIMULINK as well as for code generation with the XILINX SYSTEM GENERATOR FOR DSP. The dSPACE CONTROLDESK software is used for control and signal processing of the test bench. The drain-source voltage $v_{ds}(t)$ is directly measured and the load current $i_L(t)$ is measured with a magneto-resistive current sensor CMS3005 from SENSITEC. All measurements are sampled with 10 MSPS and 14 bit by the ADCs of the FPGA board. The input range of the ADC is ± 5 V for i_L and ± 30 V for v_{ds}. The charge and discharge current sources of the gate driver are controlled by the 14 bit, 10 MSPS DACs of the FPGA board, which exhibit a maximum output voltage of ± 10 V. The current sources provide a controllable gate-current between approximately ± 0.8 mA. Fig. 8 shows a photo of the rapid prototyping test bench.

The conducted EMI are measured with the ESPI TEST RECEIVER from ROHDE&SCHWARZ at the measurement port of the artificial network (AN) NNHV 8123-200 from SCHWARZBECK. The AN is connected between the switching load and battery voltage, according to the CSIPR 25 standard, see Fig. 7.

IV. Implementation and Measurement Results

For the following experiments, the Power MOSFET BSC020N03 is chosen to switch an ohmic/inductive load of $R_L = 2.9\,\Omega$ and $L_L = 3\,\mu$H at a battery voltage of $v_{bat} = 12.5$ V. The load represents a 55 W electric bulb in an automotive board net. The switching period is set to $T_{pwm} = 10$ ms with a duty cycle of $\chi = 0.5$. Furthermore, it

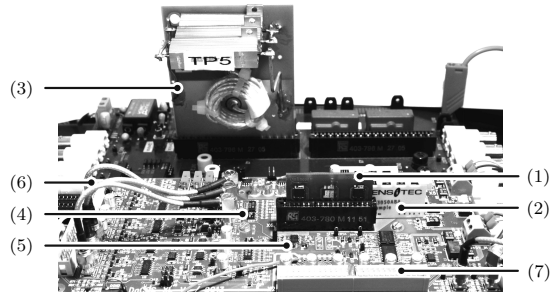

Fig. 8. Rapid prototyping test bench: (1) power MOSFET; (2) current sensor; (3) ohmic/inductive load; (4) charge current source; (5) discharge current source; (6) and (7) interface to the dSPACE system.

is assumed that the switch-on and the switch-off operation take less than $T_{sw} = 100\,\mu$s.

The necessary performance of the ADCs and DACs to achieve a proper control result was experimentally determined and yields a sampling time of $T_s = 0.5\,\mu$s and a resolution of 8 Bit, which is technically feasible with state-of-the-art low cost SoC hardware. Therefore, the resolution of the drain-source voltage and the gate current profile is diminished from 14 Bit to 8 Bit and the respective sampling time is decreased from $T_s = 0.1\,\mu$s to $T_s = 0.5\,\mu$s.

A. Implementation

The control strategies presented in Section II are implemented on the DS1005 real-time system and the DS5203 FPGA. On the FPGA, the drain-source voltage of the switch-on and switch-off operation is sampled and $N = T_{sw}/T_s = 200$ samples are stored in a buffer. After every second switching operation, the buffered samples are transferred to the real-time system, where the ILC strategy is executed. The resulting gate current profiles are transferred back to the FPGA where they are applied to the gate driver during the next switching operation.

The control parameters of both control strategies are summarized in Table I. They were determined in a two step procedure. In a first step, they were tuned by simulation experiments based on a mathematical model of the Smart Power Switch. In a second step, these parameters were applied to the test bench and fine-tuned by test bench experiments. The filter lengths of the Q-filters are set to $N_q = 8$, and

TABLE I
CONTROL PARAMETERS.

	Parameter	Value	Unit	Parameter	Value	Unit
Slew Rate	γ	1	μs/mV	f_c	0.662	MHz
S-Shape	γ_p	1	μs/mV	$f_{c,p}$	0.662	MHz
	γ_{pp}	1.5	$(\mu s)^2$/mV	$f_{c,pp}$	0.221	MHz

the length and polynomial order of the derivative filters is chosen as $N_d = 2$ and $d = 2$, respectively. The limits of

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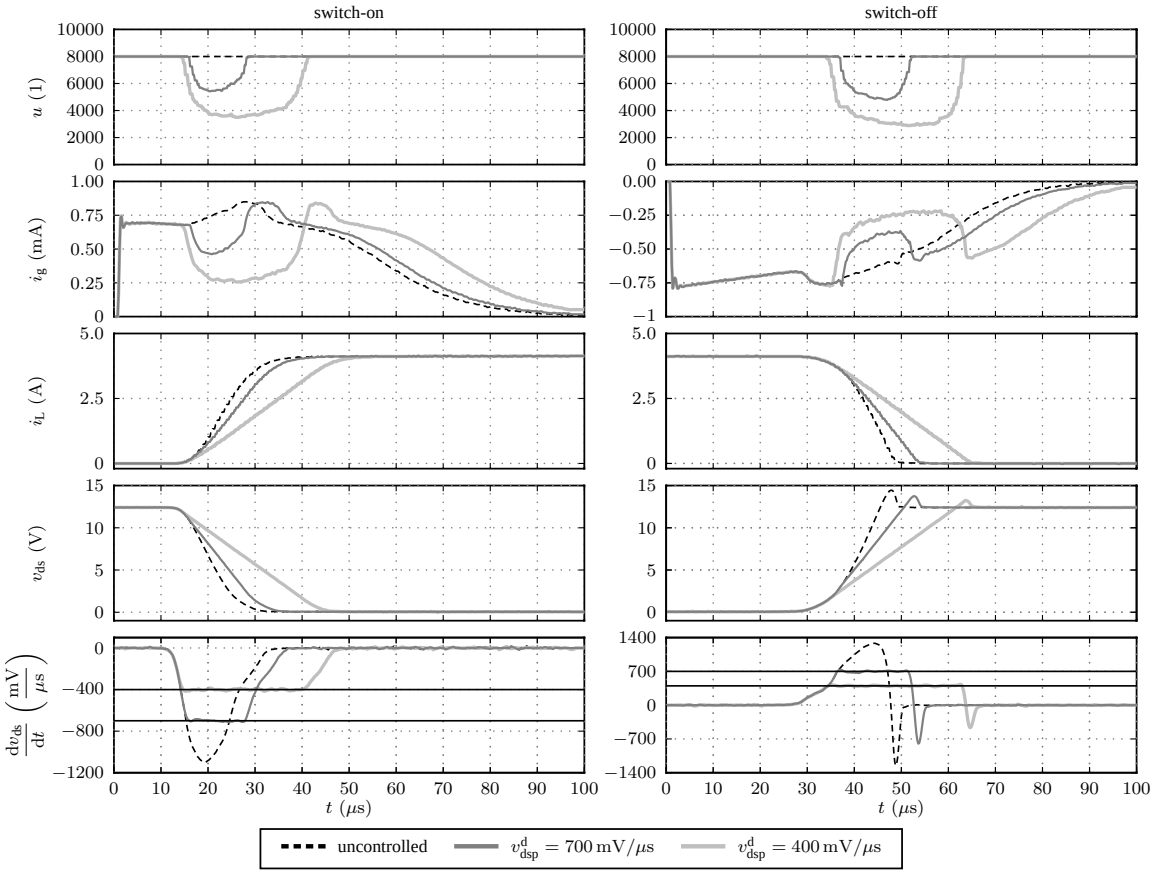

Fig. 9. Measurement results of the slew rate control strategy for different slew rate constraints.

the gate current profile are $u_{max} = 8000$ and $u_{min} = 652$ for the switch-on operation and $u_{max} = 8000$ and $u_{min} = 300$ for the switch-off operation. The limits correspond to a adjustable gate current between $\pm 0.8\,mA$. The system dead time is identified to be $1.70\,\mu s$ and is compensated by index shift of $m = 3$ of the measurement samples, i.e., $v_{ds,j}[k] = v_{ds,j}((k+3)T_s)$.

B. Measurement Results

In the following, four experimental results are presented. In the first two experiments, the slew rate is controlled to $v^d_{dsp} = 700\,mV/\mu s$ and $400\,mV/\mu s$ to investigate the influence of the slew rate constraints on EMI reduction and switching losses. The third experiment using $v^d_{dsp} = 700\,mV/\mu s$ and $v^d_{dspp} = 40\,mV/(\mu s)^2$ highlights the advantages of S-shape control compared to the pure slew rate control in terms of EMI reduction and switching losses. In the fourth experiment, the S-shape control strategy is applied to different load conditions and battery voltages to prove the proposed concept. The limits of the first and second derivatives have been chosen by tuning in order to achieve EMC according CISPR 25, Class 5.

Fig. 9 to Fig. 11 show the measurement results for the slew rate and the S-shape control strategy, respectively. All figures depict the switch-on transitions on the left side and the switch-off transitions on the right side. The gate current profiles can be found in the first row, the gate current $i_g(t)$ in the second row, the load current $i_L(t)$ in the third row, the drain-source voltage $v_{ds}(t)$ in the fourth row, and the first derivative $dv_{ds}(t)/dt$ in the fifth row. Fig. 10 and Fig. 11 additionally depict the second derivative of the drain-source voltage $d^2v_{ds}(t)/dt^2$ in row six. For a better assessment of the control performance, the range of the second derivatives are not fully shown because the uncontrolled transients exceeds the control constraints up to 50 times.

Both strategies fulfill their task of controlling the transitions of the first and/or second derivative to the constraints. The time evolution of the first derivative sticks to the respective constraint for quite a long time during the switching operation which assures maximum switching speed and minimal switching losses under the given constraints.

The second derivatives in Fig. 10 and Fig. 11 show some violations of the control constraints but the control strategy still drastically reduces the maximum amplitude of the second

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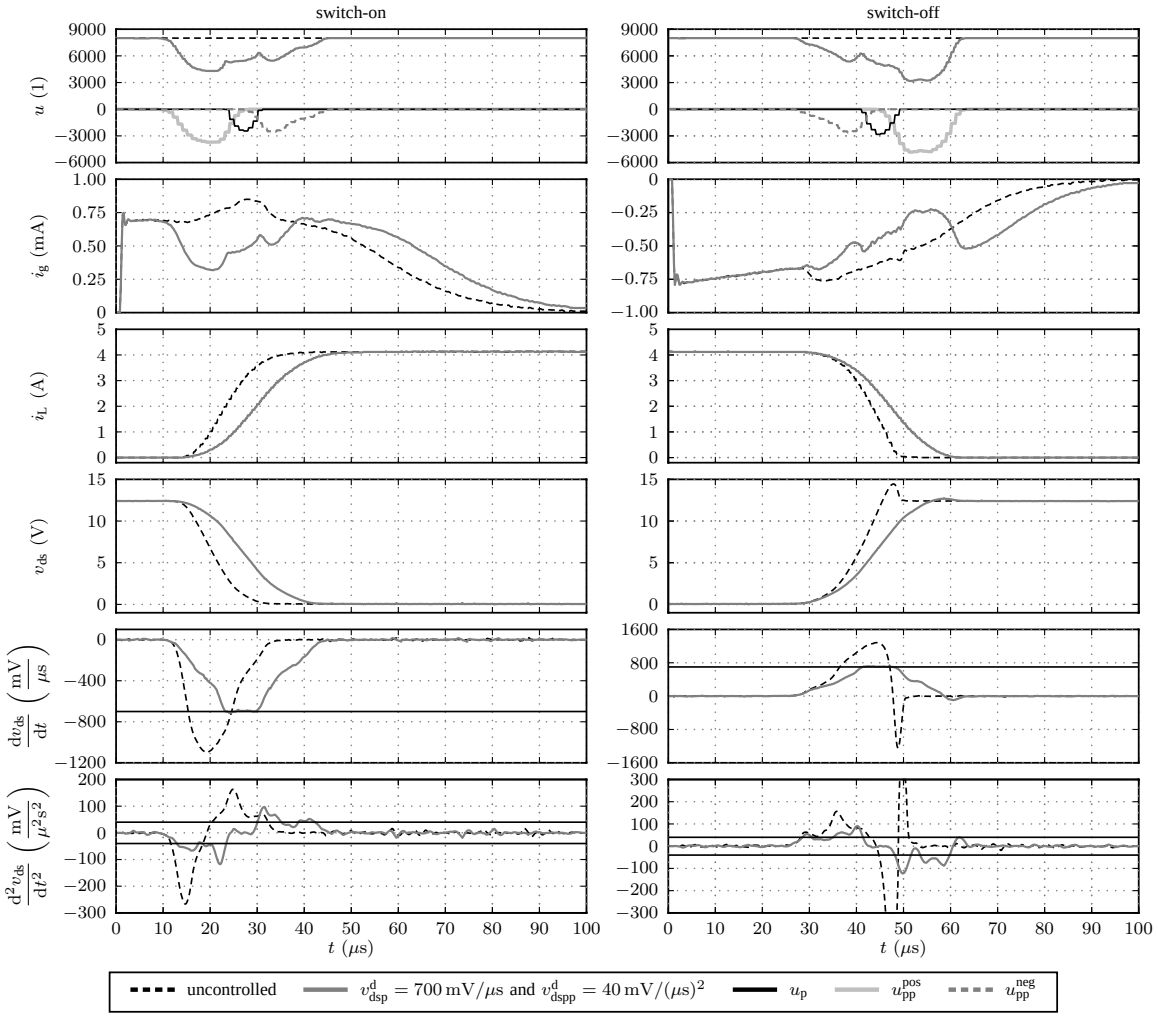

Fig. 10. Measurement results of the S-shape control strategy.

derivative. The reasons for this are twofold. On the one hand, the reduced resolution and sampling rate of the ADC causes numerical inaccuracies when calculating the second derivative of the drain-source voltage. On the other hand, it can be inferred from Fig. 10 that, in contrast to the assumptions being made, there is a small overlap of the additive gate current profiles. In the uncontrolled case, however, the second derivative reaches its absolute maximum value during the switch-off operation of about $2000\,\mathrm{mV/(\mu s)^2}$. The successful control of the slew rate also reduces the amplitude of the voltage overshoot due to inductive spiking, see $v_{ds}(t)$ in Fig. 9. An even higher reduction is achieved by the additional control of the second derivative, cf. $v_{ds}(t)$ in Fig. 10.

The application of the control strategy for different load conditions is presented in Fig. 11. It shows the specific results of the S-shape control strategy for load conditions and battery voltages in the range of $R_L = 1.8$ to $3.9\,\Omega$, $L_L = 1.8$ to $3.4\,\mu$H and $v_{bat} = 11$ to $14\,$V. The same control parameters are used for all the experiments, see Table I. The S-shape control strategy is able to adapt the gate current profile to the changed battery voltage and load condition and to control the first and second derivatives to their desired limits. Compared to the tracking of a predefined switching trajectory, an identification of load or battery parameters is not necessary and no tracking profile has to be recalculated.

Fig. 12 depicts the results of an EMC compliance test according to CISPR 25 standard as well as the occurring switching losses. To better highlight the influence of the control strategy, the results are only shown between $0.15\,$MHz and $10\,$MHz instead of the full range, i.e., $0.15\,$MHz and $30\,$MHz, according to CISPR 25. The amplitude of the EMI spectra of the uncontrolled switching transitions violates the limits of Class 5 and the test setup fails the Class 5 EMC test. The slew rate control with $v^d_{dsp} = 700\,\mathrm{mV/\mu s}$ achieves a slight reduction of

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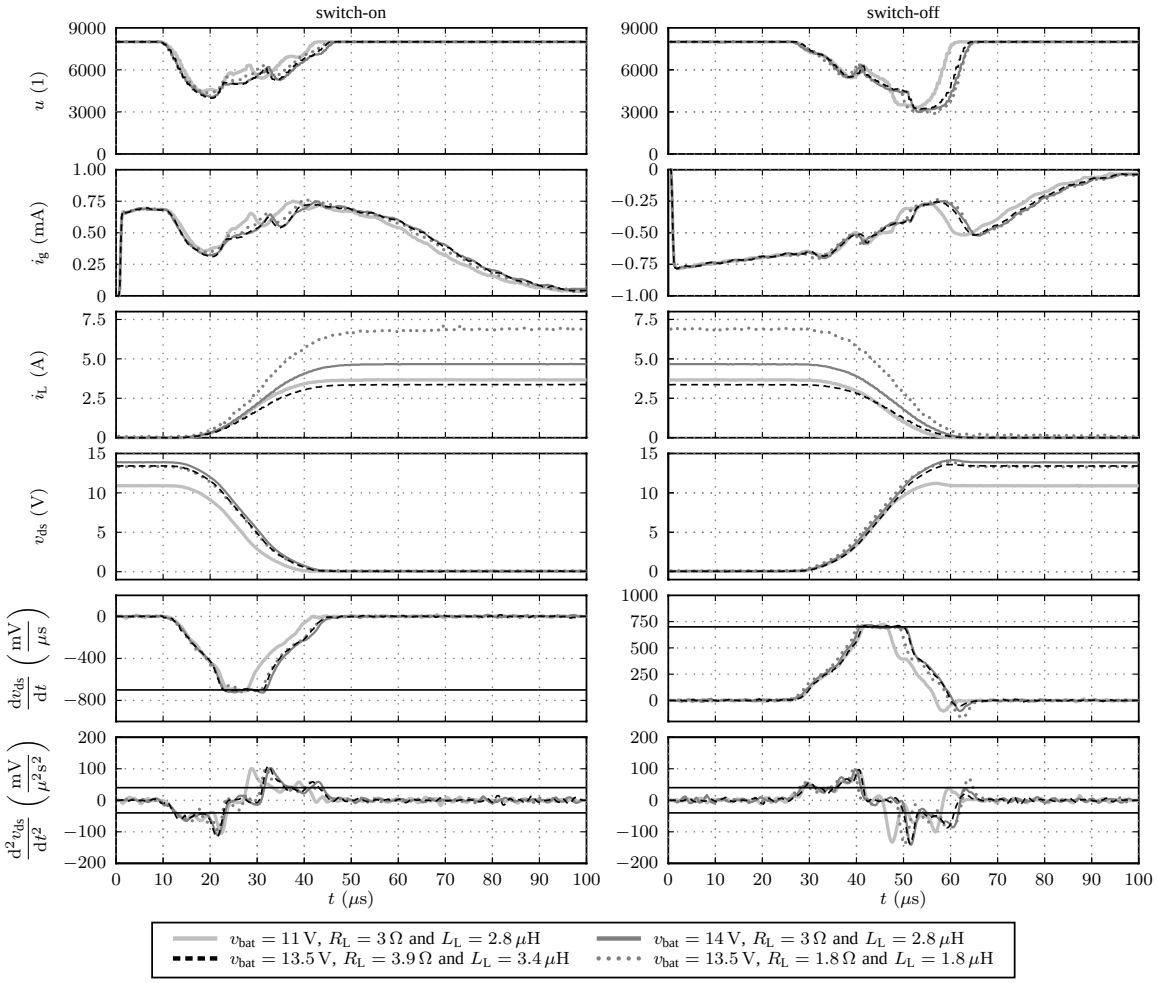

Fig. 11. Measurement results of the S-shape control strategy for load conditions and battery voltages in the range of $R_L = 1.8$ to $3.9\,\Omega$, $L_L = 1.8$ to $3.4\,\mu$H and $v_{bat} = 11$ to 14 V with the limits $v^d_{dsp} = 700\,\mathrm{mV}/(\mu\mathrm{s})$ and $v^d_{dspp} = 40\,\mathrm{mV}/(\mu\mathrm{s})^2$.

the amplitude of the EMI spectra but the Smart Power Switch still fails Class 5. A further reduction of the slew rate constraint to $v^d_{dsp} = 400\,\mathrm{mV}/\mu\mathrm{s}$ only slightly improves the results. However, the switching losses are dramatically increased so that a further decrease of the slew rate constraint is out of the question. If the second derivative is also constrained the amplitude of the EMI spectra is considerably decreased so that Class 5 level is achieved. The occurring switching losses are between the uncontrolled transitions and the slew rate control with $v^d_{dsp} = 400\,\mathrm{mV}/\mu\mathrm{s}$. The spectral peak around 2 MHz and 4 MHz is a byproduct of the sampling time of the gate current profile which is $f_s = 1/T_s = 2$ MHz.

One might expect the envelope of the spectra to be identical to the envelope of the Fourier series of an ideal trapezoidal or S-shape switching transient, see, e.g., [6]. However, this is not the case. The reason for this is threefold: First, the artificial network according to Fig. 7 in combination with the ohmic/inductive load basically behaves like a differentiator of order two in the lower frequency area, in particular from 0.15 to 1 MHz. Consequently, sharp inflection points of the switching transition result in an increased amplitude of the voltage measured at the measurement port of the AN. Second, the switching transition is not trapezoidal at all which can be seen from the measurement results of $v_{ds}(t)$ in Fig. 9 to 11. The voltage spike on $v_{ds}(t)$ due to inductive spiking leads to sharp inflection points and therefore to high EMI. Third, the EMI-receiver is based on a super heterodyne receiver and therefore applies a nonlinear operation to the measurement signal in order to determine its frequency spectra. Therefore, the spectra calculated by Fourier analysis is different from the EMI receiver measurements. Clearly, the exact shape and amplitude of the measured EMI spectra are hard to predict and cannot be directly approximated by the envelope of the Fourier series of an ideal trapezoidal or S-Shape switching transition.

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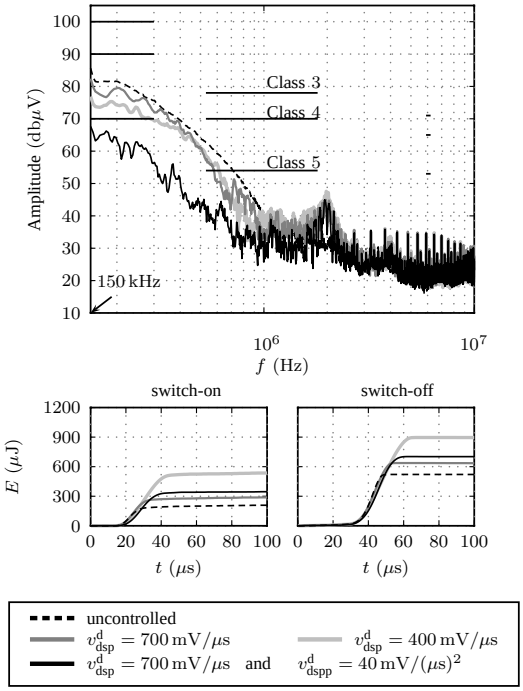

Fig. 12. Measurement results of the EMC compliance test according to CSIPR 25 with the EMI-Receiver settings: $f_{\mathrm{RBW}} = 9\,\mathrm{kHz}$, $f_{\mathrm{VBW}} = 90\,\mathrm{kHz}$, $f_{\mathrm{STEP}} = 4\,\mathrm{kHz}$ and $T_{\mathrm{DWELL}} = 50\,\mathrm{ms}$ and the corresponding switching losses.

Concerning the trade-off between EMI reduction and switching losses, the simple slew rate control strategy is able to reduce the spectral EMI amplitude but the Smart Power Switch still does not pass the Class 5 test. A further reduction of the slew rate constraint and therefore of the EMI level is not feasible because of the increasing switching losses. With the S-shape strategy, Class 5 is passed with a moderate increase of the switching losses and therefore this concept clearly constitutes a good compromise between EMI reduction and switching losses.

V. Conclusion

In this paper, a digital adaptive feedforward slew rate control strategy and its extension to an S-Shape control was presented. Both control strategies are based on a feedforward gate current profile which is adapted from switching cycle to switching cycle by an Iterative Learning Control strategy in order to account for model uncertainties, load variations and temperature dependencies. A rapid prototyping test bench was presented, and the performance and robustness of the control strategies were demonstrated by a series of measurement results. By the proposed control concepts it is possible to control the first and/or second derivative of the switching transient to the desired limits. With this, maximum switching speed and minimal switching losses can be achieved. The strategy controls the first and second derivative independently from the switching characteristics of the power switch, the load conditions and battery voltage. Furthermore, the control strategy is robust against variations of the load and battery voltage which is a great benefit compared to the tracking of a switching profile. Furthermore, an EMC compliance test according to the CSIPR 25 standard was preformed. The EMC performance can be improved by the slew rate control however, the additional control of the second derivative yields to a good trade-off between EMI reduction and switching losses. Since the presented strategy is digitally implemented it can be simply reused for different power switches and loads. For the considered case of the Smart Power Switch, a suitable SoC hardware has to have ADCs and DACs with at least a sampling rate of 2 MSPS and a resolution of 8 Bit to achieve a good control result. Future work will be concerned with the proof of convergence of the control strategy and the improvement of the convergence speed.

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