EMI Reduction for Smart Power Switches by Iterative Tracking of a Gaussian-shape Switching Transition

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EMI Reduction for Smart Power Switches by Iterative Tracking of a Gaussian-shape Switching Transition

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Abstract

This paper presents a digital control strategy to track a Gaussian reference switching profile at the output voltage of a Smart Power Switch by a feedforward gate current profile. The gate current profile is adapted from switching cycle to switching cycle by an Iterative Learning Control strategy to compensate for model inaccuracies, load variations and temperature dependencies. The presented strategy reduces the generation of conducted electromagnetic interferences in a power optimal way. The strategy is verified by a series of measurement results on a rapid prototyping test bench and by an EMC compliance test according to CISPR 25.

1. Introduction

Smart Power Switches are power switches with integrated control and protection functions for the switching of middle and high current loads in industrial and automotive applications [1, 2]. In the considered case of the Smart Power Switch, the rapid switching generates conducted broadband disturbances up to $2\,\mathrm{MHz}$. These electromagnetic interferences (EMI) have to be limited in order to meet the demands on electromagnetic compatibility (EMC). A common method to reduce the conducted EMI is the application of EMI-filters [3]. However, EMI-filters are bulky and cannot be integrated on the chip of the Smart Power Switch. Moreover, in particular in automotive applications the EMI filters constitute unwanted additional parts on the circuit board because they cause additional costs, space requirements and weight. Therefore, the generation of EMI has to be prevented by other measures, for instance by the active control of the switching transients [4, 3, 5].
Up to now, mostly analog control strategies are applied to control the switching transients, e.g., they control the maximum slew rate of the output voltage or the load current [6]. This slew rate limitation strategies reduce the EMI generation due to the reduction of high frequency components but also lead to an unnecessary increase of the switching losses. Since Smart Power Switches have to be operated without additional heat sinks or other cooling methods due to space and weight requirements, the switching losses are of major concern. A better trade-off between EMI reduction and occurring switching losses is achieved by the limitation of higher order derivatives [3, 5]. According to [7], a Gaussian switching profile accomplishes the optimal tradeoff between switching losses and reduction of high frequency components of the output voltage, and therefore the reduction of EMI. In [4], an analog control strategy is proposed to track a Gaussian reference transition. Analog control strategies are designed for certain load conditions and power classes and are hardly reusable for different circuit designs and applications without a major redesign.

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The advent of cheap and powerful system-on-chip solutions allows to overcome these disadvantages by a digital implementation of the control strategy. A digital implementation not only reduces development costs and time to market. It also enables the application of advanced control strategies such as nonlinear and adaptive control strategies. Recently, a few digital control strategies have been presented [8, 9] and [10, 11]. In these works, adaptive gate current profiles are used to control and limit the slew rates of the switching transients. Adaptive feedforward control strategies have the potential to systematically account for dead times in the system and to compensate for model inaccuracies, temperature dependencies and load variations.
In this paper, a desired switching transition is tracked using a highly resolved adaptive gate current profile. The gate current profile is adapted by an Iterative Learning Control (ILC) strategy. Furthermore, the desired switching transition is designed by a trajectory generator depending on the supply condition of the Smart Power Switch. The presented control strategy is verified by a series of measurement results on a rapid prototyping test bench and by an EMC compliance test according to CISPR 25 [12]. The results show that the EMI can be power efficiently reduced by the proposed concept.

2. Control Strategy

For the sake of brevity only the control strategy for the switch-on operation is presented in the following. However, the strategy is applicable to the switch-off operation in the same way.

The basic idea of the control strategy is that a desired switching trajectory, e.g., a desired output voltage transition, is tracked using an adaptive feedforward gate current profile. To compensate the deviations from the desired switching trajectory, the gate current profile is adapted from switching cycle to switching cycle by an Iterative Learning Control (ILC) strategy. ILC is rewarding for systems which execute a task multiple times, see, e.g., [13, 14]. In this case, the tracking error between the desired and the actual switching transition can be minimized from one switching operation to the next. A block diagram of the proposed control strategy is depicted in Fig. 1.

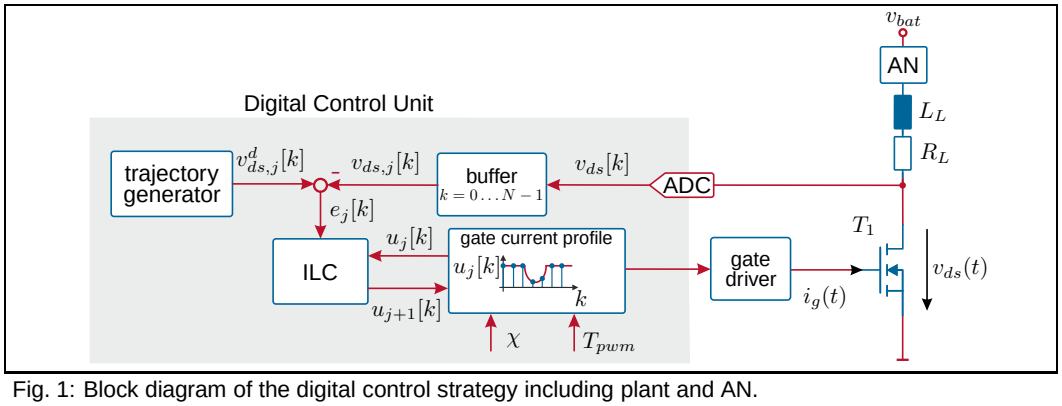

Fig. 1: Block diagram of the digital control strategy including plant and AN.

It consists of the digital control unit and the plant. The digital control unit might be a μC or an FPGA. The plant itself comprises the gate driver, the analog-to-digital converter (ADC), the

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power switch T_1 and the ohmic/inductive switching load L_L and R_L. The plant is supplied with the battery voltage v_{bat} using an artificial network (AN) according to CISPR 25. The power switch operates in PWM-mode with the modulation periode T_{pwm} and a duty cycle of χ. The switching operation itself is controlled by a highly resolved gate current profile, $u_j[k] = u_j(kT_s)$, where j denotes the iteration index and $k = 0, \ldots, N-1$ the sampling index. The profile is sampled with the sampling time T_s and N samples are stored in a buffer of the digital control unit. Further, $u_j[k]$ is applied to the power switch using a digitally controllable gate driver. The corresponding drain-source voltage of the power switch, $v_{ds}(t)$, is measured, sampled with T_s and N samples are also stored in a buffer, i.e., $v_{ds}[k] = v_{ds}((k+m)T_s)$. Note that the samples of v_{ds} are shifted by m in order to account for system dead times.
The trajectory generator generates the desired reference switching trajectory $v^d_{ds,j}[k]$ depending on the actual supply condition. An appropriate initial gate current profile, $u_0[k]$, can, e.g., be determined by solving an optimal control problem [15].

2.1. Iterative Learning Control Strategy

As previously mentioned, the switching operation is controlled by the gate current profile $u_j[k]$. The profile is composed of its constant maximum value u_{max} and the adaptive profile $u_{g,j}[k]$, i.e.,

$$u_{j+1}[k] = u_{max} + u_{g,j+1}[k]. \tag{1a}$$

By applying u_{max} to the gate driver, maximum switching speed and therefore minimal switching losses are achieved. Deviations from the desired switching trajectory, i.e., the tracking error

$$e_j[k] = v^d_{ds,j}[k] - v_{ds,j}[k], \tag{1b}$$

are compensated by the adaptive profile. Therefore, $u_{g,j}[k]$ is iteratively adapted from one switching operation to the next by the following ILC law

$$\bar{u}_{g,j+1}[k] = q[k] * \left(u_{g,j}[k] + \gamma e_j[k]\right), \tag{1c}$$

where $*$ denotes the discrete convolution operator, γ the constant learning gain and $q[k]$ the impulse response of the so-called Q-filter [14]. To take into account the physical limitation of the gate driver and consequently the gate current $i_g(t)$, the saturation function

$$\begin{aligned} u_{g,j+1}[k] &= \operatorname{sat}\Big(\bar{u}_{g,j+1}[k], 0, -u_{max} + u_{min}\Big) \\ &= \begin{cases} 0, & \bar{u}_{g,j+1}[k] > 0 \\ \bar{u}_{g,j+1}[k], & -u_{max} + u_{min} \le \bar{u}_{g,j+1}[k] \le 0 \\ -u_{max} + u_{min}, & \bar{u}_{g,j+1}[k] < -u_{max} + u_{min} \end{cases} \end{aligned} \tag{1d}$$

is applied. Here, u_{min} and u_{max} are the lower and upper limit of the gate current profile, respectively. In order to avoid the learning of non-repetitive disturbances and noise, the adapted profile is filtered with the Q-filter $q[k]$. In literature, e.g., [16], a Gaussian distribution

$$g(t) = \frac{1}{\sigma_q \sqrt{2\pi}} \exp\left(-\frac{t^2}{2\sigma_q^2}\right) \tag{2}$$

with the standard derivation σ_q is often used as non causal, zero phase Q-filter. To obtain such a Q-filter, the Gaussian function (2) is discretized

$$g[k] = \frac{T_s}{\sigma_q \sqrt{2\pi}} \exp\left(-\frac{k^2}{2\sigma_q^2}\right), \qquad k \in \mathbb{N} \tag{3a}$$

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windowed with a rectangular window of length $2N_q + 1$ and normalized, i.e.,

$$q[k] = \frac{g[k]}{\sum_{m=-N_q}^{N_q} g[m]} \qquad \text{for} \qquad k \leq |N_q|. \tag{3b}$$

The standard derivation σ_q is related to the tunable 3-dB filter bandwidth f_c by

$$\sigma_q = \frac{\sqrt{\ln(2)}}{2\pi f_c}. \tag{3c}$$

The robustness and convergence speed of the control strategy can be influenced by the learning gain γ and the 3-dB bandwidth of the Q-filter f_c. A high value of γ increases the convergence speed but decreases the robustness. Similarly, a high bandwidth f_c tends to reduce the convergence error but also weakens the robustness, see, e.g., [16, 17].

2.2. Trajectory Generator

In principle, any appropriate switching profile could be used as desired switching transition. However, according to [7], a Gaussian switching transition achieves the optimal trade-off between switching speed and reduction of high frequency components. Such a Gaussian-shape trajectory is generated by the function

$$v_{ds,j}^{d}[k] = \begin{cases} \bar{v}_{bat}, & k < k_s \\ \bar{v}_{bat} - v_g[k - k_s]\left(\bar{v}_{bat} - \bar{v}_{ds_{on}}\right), & k_s \leq k \leq k_e \\ \bar{v}_{ds_{on}}, & k > k_e \end{cases}. \tag{4a}$$

Herein, $\bar{v}_{bat}$ denotes the average battery voltage, and $\bar{v}_{ds_{on}}$ the average on-voltage. Both voltages can either be set to an appropriate constant value or determined from the latest measurements of the drain-source voltage. Furthermore, k_s and k_e indicate the start and end index of the switching trajectory, and v_g denotes the discrete step response of the Gaussian filter kernel (3a) with $\sigma_q = \sigma_v$, i.e.,

$$v_g[k] = h[k] * g[k - k_{sw}/2]. \tag{4b}$$

Herein, $h[k]$ denotes the Heaviside function and $k_{sw} = k_e - k_s + 1$ the sampling size of the Gaussian switching trajectory. The switching trajectory starts at k_s in order to account for the turn on delay of the switching operation due to the charging of the input capacitances of the power switch.
The free design parameters of the trajectory are the truncation error of the Gaussian filter kernel (2), i.e., $\Delta_g = g\left(t_{sw}/2\right)\left(\bar{v}_{bat} - \bar{v}_{ds_{on}}\right)$ with $t_{sw} = k_{sw}T_s$, and the maximal slew rate of the switching transient, $v_{dsp,max} = g\left(0\right)\left(\bar{v}_{bat} - \bar{v}_{ds_{on}}\right)$. Using these parameters, the duration of the Gaussian switching profile calculates as

$$k_{sw} = \left\lceil \frac{T_s}{t_{sw}} \right\rceil = \left\lceil \frac{2}{T_s}\sigma_v \sqrt{-\ln\left(\frac{2\pi\Delta_g^2\sigma_v^2}{(\bar{v}_{bat} - \bar{v}_{ds_{on}})^2}\right)} \right\rceil \tag{5}$$

with

$$\sigma_v = \frac{\bar{v}_{bat} - \bar{v}_{ds_{on}}}{v_{dsp,max}\sqrt{2\pi}}. \tag{6}$$

The operator $\lceil \cdot \rceil$ indicates the integer rounding towards plus infinity.

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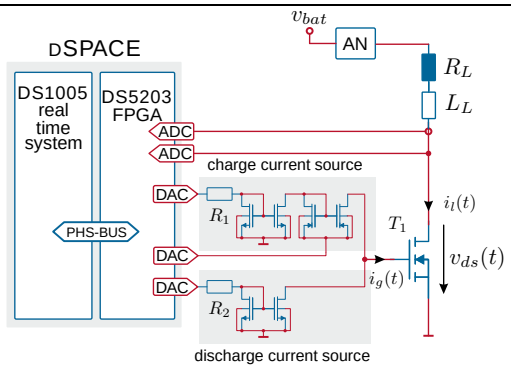
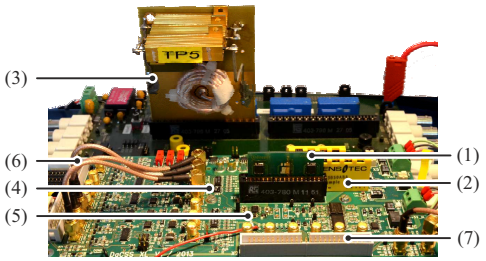
3. Rapid Prototyping Test Bench

Fig. 2 depicts the block diagram and a picture of the rapid prototyping test bench. It consists



((a)) Block diagram of the rapid prototyping test bench.



((b)) Rapid prototyping test bench: (1) power switch; (2) current sensor; (3) ohmic/inductive load; (4/5) charge/discharge current source; (6/7) interface DSPACE.

Fig. 2: Block diagram of the rapid prototyping test bench.

of the DSPACE real-time measurement and control system DS1005 PPC with the DS5203 FPGA extension board, the power switch T_1 and the ohmic/inductive switching load R_L and L_L. A digitally controllable charge and discharge current source serves as gate driver. The current sources are controlled by the $14\,\mathrm{bit}, 10\,\mathrm{MSPS}$ DACs of the FPGA board and provide a controllable gate current approximately in the range of $\pm 0.8\,\mathrm{mA}$. The load current $i_l(t)$ and the drain-source voltage $v_{ds}(t)$ are first measured and then discretized by the $14\,\mathrm{bit}$, $10\,\mathrm{MSPS}$ ADCs of the FPGA extension board. The test bench is supplied with the battery voltage v_{bat} using an artificial network (AN) according to the CSIPR 25 standard which is used to measure the conducted EMI.

4. Implementation and Measurement Results

For the following experiments, the power MOSFET BSC020N03 is used to switch a load of $R_L = 2.9\,\Omega$, and $L_L = 3\,\mu\mathrm{H}$ with the battery voltage of $v_{bat} = 12.5\,\mathrm{V}$. The MOSFET is operated in PWM-mode with $T_{pwm} = 10\,\mathrm{ms}$ and $\chi = 0.5$. The sampling rate of the ADC and DAC has been artificially reduced from $10\,\mathrm{MSPS}$ to $2\,\mathrm{MSPS}$ and the resolution of the ADC and DAC from $14\,\mathrm{bit}$ to $10\,\mathrm{bit}$ to simulate state-of-the-art low cost SOC hardware. Furthermore, it is assumed that the switching operation takes no longer than $100\,\mu\mathrm{s}$. Thus, the length of the gate current profile is determined to be $N = 200$.
The following EMC test results have been performed using the ESPI TEST RECIEVER from ROHDE & SCHWARZ and the artificial network NNHV 8123-200 from SCHWARZBECK.

4.1. Control Parameters

The window size of the Q-filter (3) is set to $N_q = 9$ and the 3-dB bandwidth is experimentally chosen as $f_c = 0.132\,\mathrm{MHz}$ for the switch-on and switch-off operation. Furthermore, the learning

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gain (1c) is set to $\gamma^{\text{on}} = -1$ and $\gamma^{\text{off}} = 1$. The system dead time is determined to be $1.5\,\mu\text{s}$ and therefore the measurement vector of v_{ds} is shifted by $m = 3$. The limits of the gate current profile, see (1d), are set to $u_{max} = 9.76\,\text{V}$ and $u_{min} = 0.8\,\text{V}$ for the switch-on operation and $9.76\,\text{V}$ and $u_{min} = 0.4\,\text{V}$ for the switch-off operation. Note that the gate current profile is in volt because the charge and discharge current sources are controlled by the output voltage of the DAC of the dSPACE system. In the experiments, the desired switching trajectories (4) are designed for different maximal slew rates with a truncation error of $\Delta_g = 10\,\text{mV/s}$ and the starting index $k_s^{\text{on}} = 4$ and $k_s^{\text{off}} = 8$.

4.2. Measurement Results

Fig. 3 ((a)) shows the time domain measurement results for the uncontrolled and controlled switching operations. The left hand side depicts the results for the turn-on operation and the right hand side for the turn-off. The gate current profiles can be found in the first row. The second row shows the drain-source voltage $v_{ds}(t)$ (solid line) together with the desired switching profile $v_{ds}^d(t)$ (dashed line). Furthermore, the control error $e = v_{ds}^d - v_{ds}$ is depicted in the third row. The last two rows show the first derivative of $v_{ds}(t)$ and $v_{ds}^d(t)$ and the time evolution of the switching losses. The maximal control error for both desired trajectories is only about $25\,\text{mV}$. Thus, it is evident that the presented strategy is able to track a desired switching trajectory within the given specifications. The corresponding results of the EMC compliance test can be found in Fig. 3 ((b)). The uncontrolled switching operation violates the limits of Class 4 and thus fails the Class 4 EMC test. In contrast, the EMI amplitudes of the controlled switching operations are far below the Class 5 limits and easily fulfill the highest EMC requirements. By reducing the maximal slew rate of the trajectories from $850\,\text{mV}/\mu\text{s}$ to $700\,\text{mV}/\mu\text{s}$, the spectral amplitude can only be partially lowered whereas the switching losses increase significantly. In contrast to the uncontrolled case, the controlled switching transitions exhibit a spectral peak at $2\,\text{MHz}$ and $4\,\text{MHz}$. This spectral peak is a byproduct of the sampling of the gate current profile. However, the EMI level generated by the sampling frequency of the gate driver is low enough to not cause any EMI problems. However, the influence of the samplling time still has to be considered for a future circuit design so that the control circuit itself does not become the source of disturbing EMI.

5. Conclusion

In this paper, a digital control strategy was presented that tracks a desired switching trajectory at the output terminal of a Smart Power Switch. The strategy is based on an adaptive feed-forward gate current profile which is iteratively adapted by an ILC strategy in order to handle model uncertainties due to fabrication tolerances, load variations and temperature dependencies. The performance and robustness of the proposed approach were demonstrated by test bench measurements and an EMC compliance test. The measurement results show that the strategy is able to track the desired switching trajectory and to reduce the spectral amplitude of the conducted EMI far below the required levels of the CISPR 25 standard.

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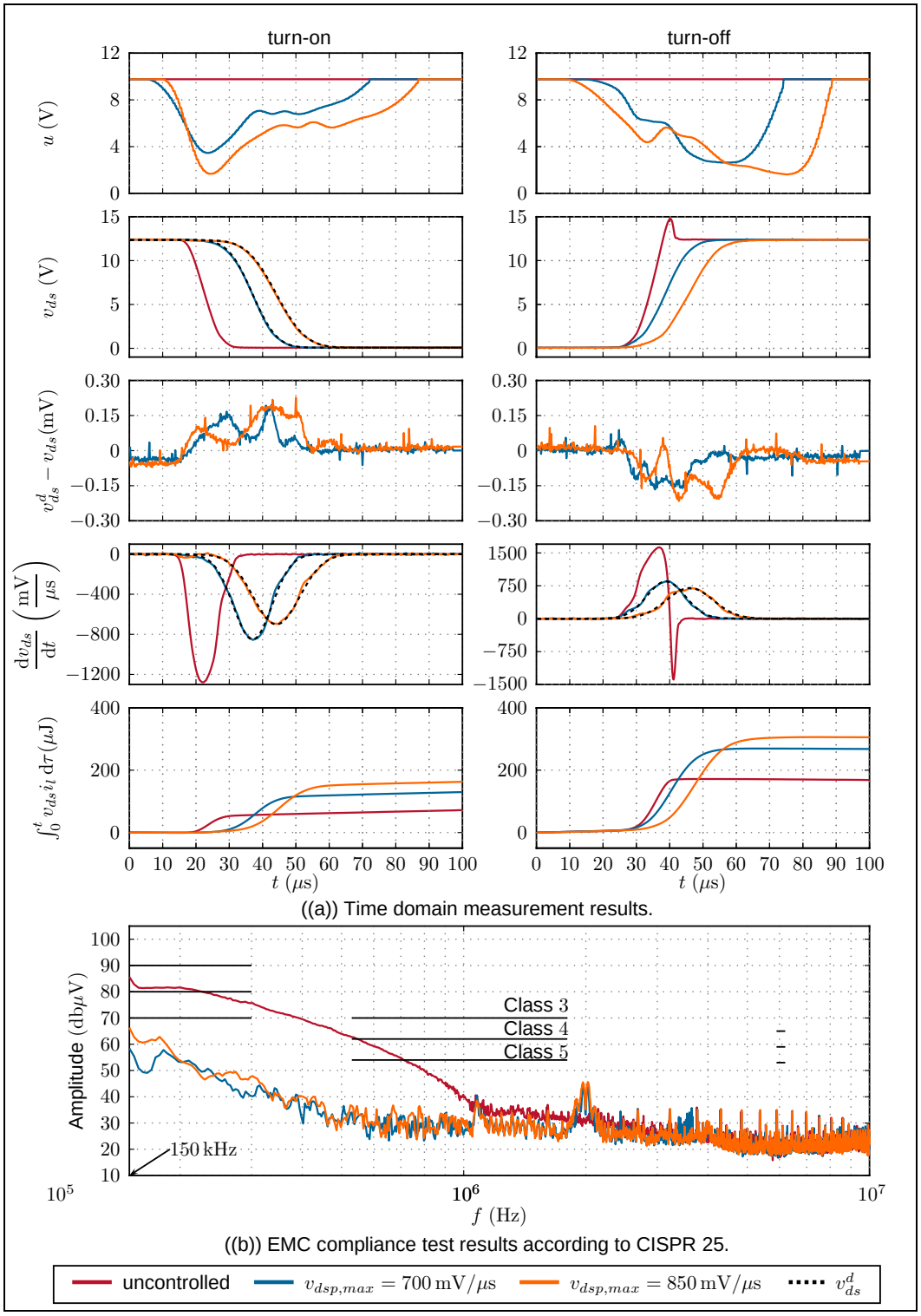

Fig. 3: Measurement results for the switching profiles with different maximal slew rates.

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