Mathematical Modeling and Analysis of a Very Low Frequency HV Test System

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and published in *IEEE Transactions on Power Electronics.*

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Mathematical Modeling and Analysis of a Very Low Frequency HV Test System

Stefan Eberharter, Wolfgang Kemmetmüller, *Member, IEEE,* and Andreas Kugi, *Member, IEEE,*

***Abstract*—This paper presents a new type of very low frequency (VLF) high-voltage test system for on-site cable tests up to 200 kV rms. The VLF system is based on a so called Differential Resonance Technology (DRT), which enables a light-weight and compact construction of cable test systems. A mathematical model of the test system is presented, which is used for a detailed analysis and optimization of the DRT system. Measurement results on a prototype for 200 kV rms and loads up to 0.75 µF are used to validate the mathematical model and to show the feasibility of the test system.**

***Index Terms*—cable testing, on-site testing, high-voltage, very low frequency, mathematical modeling**

I. Introduction

In recent years, a forced expansion of regenerative energy production by means of large scale wind parks and photovoltaic power plants can be observed. These mostly decentralized systems are often connected to the electricity distribution network by high- and ultra-high-voltage cables. These cables allow transmissions with voltages of 500 kV and higher and are usually buried in the ground or sea floor.

In order to guarantee a fail-safe energy supply, the cables have to pass strict quality tests. Beside factory acceptance tests of newly produced cables, suitable test methods and devices are needed for quality and failure testing of already installed cables.

Because of the large capacitance of the high- and ultra-high-voltage cables, the test devices have to generate a high amount of reactive power, which is directly reflected in a large size and weight of classical test devices [1]. For on-site tests of already installed cables it is, however, important that the test devices exhibit a compact and light-weight design.

Therefore, a new type of cable test method using very low frequencies (VLF) in the range of 0.01 Hz to 0.1 Hz has been established in the recent years, see [2]–[7]. The substantial reduction of the test signal frequency compared to the power frequency results in a drastic reduction of the required reactive power. This in turn enables the construction of more compact and light-weight cable test systems. For VLF testing of mid- and high-voltage cables up to 80 kV rms, several test systems are already available [8]–[12]. Some of these mid- and high-voltage test systems use voltage multiplier circuits, as given in [13], [14], for the generation of the high-voltage test signals. The use of voltage multipliers allow a very compact and light-weight design of the test systems, however, they also limit the maximum output voltage of the test signal to a lower voltage level. Thus, VLF cable test systems for cables of higher voltage classes beyond 100 kV are still very rare.

In this paper, a new type of VLF test system, extending the range of mobile cable test systems to higher voltages, will be introduced. This new VLF system is based on the so called Differential Resonance Technology (DRT) [15]–[17], which allows cable tests with voltages up to 800 kV rms and output frequencies in the range of 0.01 Hz up to 10 Hz. The desired frequency of the output test signal can be easily adjusted by changing the frequencies of the input signals of the system. In order to accurately control the amplitude and shape of the test voltage, a suitable control strategy is required. The mathematical model derived in this manuscript represents the basis for this controller design. Moreover, important conclusions for the dimensioning of the system parameters and the dynamic behavior of the system can be drawn based on an analysis of the mathematical model.

The paper is organized as follows: Section II gives an overview of the DRT system set-up and its functional principle. It is followed by the development of a mathematical model in Section III. Measurement and simulation results are depicted in Section IV. Subsequently, in Section V, the DRT system will be analyzed based on different simulation studies. Conclusions are drawn in Section VI.

II. DRT system overview

Fig. 1 depicts the basic working principle of the DRT system. The main components of the system are the power module, which generates the two input voltages u_{p1} and u_{p2} of the exciter transformer, the series resonant circuit, the demodulator (switched valve unit - SVU) and the capacitive/resistive load.

The resonant circuit is excited at its resonant angular frequency ω_r by the two output voltages u_{p1} and u_{p2} of the power module. These voltages are pulse-width-modulated signals with a constant amplitude of approximately 540 V, generated by two full-bridges. The high quality factor Q of the serial resonant circuit yields the very high resonant voltage u_r at the resonator capacitor, which is needed for the testing of high-voltage cables. If the angular frequencies ω_{p1} and ω_{p2} of u_{p1} and u_{p2} are chosen as $\omega_{p1} = \omega_r - \omega_\Delta$ and $\omega_{p2} = \omega_r + \omega_\Delta$, respectively, the resonant voltage u_r results in an amplitude modulated high-voltage signal of the form $u_r = \hat{u}_r \sin(\omega_\Delta t) \sin(\omega_r t)$.

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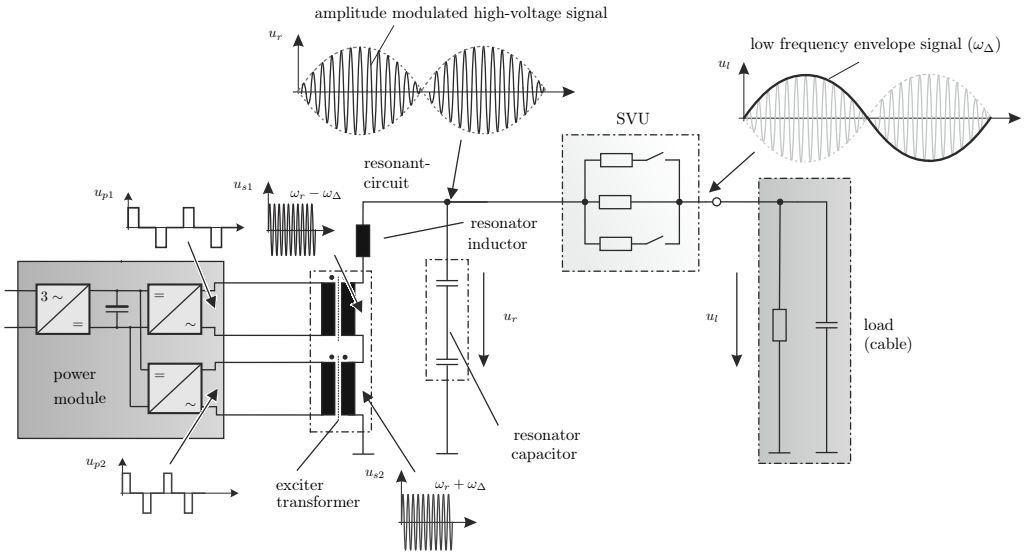

Fig. 1. Functional principle of the DRT test system.

This high-voltage signal comprises a high carrier angular frequency ω_r and a sinusoidal envelope signal with a low differential angular frequency ω_Δ. The angular frequency ω_Δ of the envelope signal can be easily changed by adjusting the modulation frequency of the power module voltages.

The sinusoidal low frequency envelope of the resonant voltage u_r is demodulated by the demodulator (SVU), such that the desired low frequency high-voltage u_l is generated at the load, i.e. the cable to be tested. A simplified schematic of the SVU is illustrated in Fig. 2. The SVU comprises N modules, whereas each module consists of 5 SVU boards. The choice of 5 SVU boards for each SVU module was made due to the maximum admissible voltage of the switching elements and the geometric constraints of the installation size. The switching elements of the demodulator circuits are high-voltage thyristors. Each thyristor has a serial low-ohmic loading resistor R_{lo} and a parallel high-ohmic discharge resistor R_d. A capacitor C_{dm} connected in parallel to each SVU board is used to guarantee a homogeneous distribution of the voltage along the different modules of the SVU, see the discussion in Section III-B. Each module can be controlled individually in that sense that all thyristors of the negative or positive branch are either turned on or off.

By a suitable switching of the thyristors, the effective resistance of the overall demodulator can be adjusted such that the high frequency resonant voltage is demodulated. The energy required for the switching of the thyristors is extracted from the high carrier frequency voltage across each SVU board, see Fig. 2. This energy recovery circuit affects the behavior of the SVU and must therefore be taken into account in the mathematical model.

The intended testing frequency of the DRT system lies in the range of 0.01 Hz up to 0.1 Hz, where higher frequencies require increased power of the power module. This fact limits

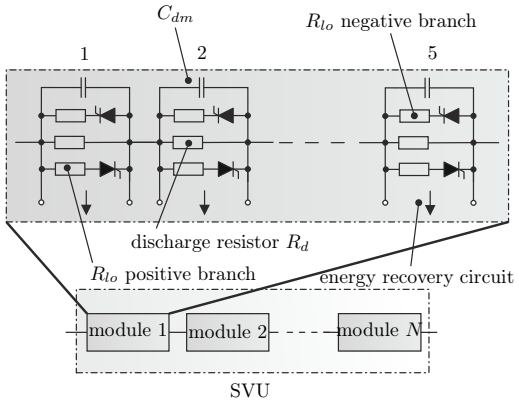

Fig. 2. Simplified schematic of the demodulator (SVU).

the maximum capacity C_l of the cables to be tested at a certain test frequency.

III. Mathematical Modeling

The mathematical model is the basis for the analysis and the optimization of the system behavior. Furthermore, the mathematical model allows the simulation of different system configurations and control strategies.

In a first step, the basic model introduced in [17], is extended to describe the main components and the operating principle of the DRT system in Section III-A. In order to analyze the influence of e.g. the energy recovery circuit or stray capacitances on the system behavior, a further expansion of the mathematical model is presented in Section III-B and III-C.

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A. Basic model

A simplified equivalent circuit diagram of the DRT system described in Section II is shown in Fig. 3. The basic model

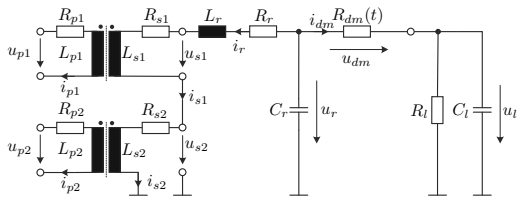

Fig. 3. Circuit diagram of the DRT test system with a continuously adjustable demodulator resistor $R_{dm}(t)$.

relies on the simplification that the overall demodulator can be described by a continuously variable resistor $R_{dm}(t)$. The value of $R_{dm}(t)$ can be varied between R_{on} (value of $5NR_{lo}$) and R_{off} (value of $5NR_d$).

The exciter transformer is supplied by the tunable voltages of the power module u_{p1} and u_{p2}. Faraday's law applied to the first exciter coil yields

$$L_{p1}\frac{\mathrm{d}\,i_{p1}}{\mathrm{d}\,t} + L_{ps1}\frac{\mathrm{d}\,i_{s1}}{\mathrm{d}\,t} = -R_{p1}i_{p1} + u_{p1} \tag{1a}$$

$$L_{ps1}\frac{\mathrm{d}\,i_{p1}}{\mathrm{d}\,t} + L_{s1}\frac{\mathrm{d}\,i_{s1}}{\mathrm{d}\,t} = -R_{s1}i_{s1} + u_{s1}, \tag{1b}$$

with the inductance L_{p1}, the current i_{p1} and the resistance R_{p1} of the primary side, as well as the current i_{s1}, the resistance R_{s1} and the inductance L_{s1} of the secondary side of the transformer. The inductance L_{ps1} describes the coupling between the primary and secondary coil of the exciter transformer and is calculated by

$$L_{ps1} = k_1\sqrt{L_{p1}L_{s1}}, \tag{2}$$

with the coupling factor $0 < k_1 < 1$.

Similar to the first exciter coil the mathematical equations of the currents i_{p2} and i_{s2} result in

$$L_{p2}\frac{\mathrm{d}\,i_{p2}}{\mathrm{d}\,t} + L_{ps2}\frac{\mathrm{d}\,i_{s2}}{\mathrm{d}\,t} = -R_{p2}i_{p2} + u_{p2} \tag{3a}$$

$$L_{ps2}\frac{\mathrm{d}\,i_{p2}}{\mathrm{d}\,t} + L_{s2}\frac{\mathrm{d}\,i_{s2}}{\mathrm{d}\,t} = -R_{s2}i_{s2} + u_{s2}, \tag{3b}$$

with the second coupling inductance

$$L_{ps2} = k_2\sqrt{L_{p2}L_{s2}}, \quad 0 < k_2 < 1. \tag{4}$$

The electric circuit depicted in Fig. 3 shows that the secondary currents i_{s1} and i_{s2} have to meet the equation $i_{s1} = i_{s2} = i_r$, where i_r is the current through the resonator inductor L_r. Thus, the differential equation of the resonator current i_r reads as

$$L_{ps1}\frac{\mathrm{d}\,i_{p1}}{\mathrm{d}\,t} + L_{ps2}\frac{\mathrm{d}\,i_{p2}}{\mathrm{d}\,t} + (L_{s1} + L_{s2} + L_r)\frac{\mathrm{d}\,i_r}{\mathrm{d}\,t} = -(R_{s1} + R_{s2} + R_r)\,i_r + u_r, \tag{5}$$

where R_r is the resistance of the resonator circuit and u_r is the voltage across the resonator capacitor C_r. Further, the resonator voltage is described by

$$\frac{\mathrm{d}\,u_r}{\mathrm{d}\,t} = \frac{1}{C_r}\left(-i_r - i_{dm}\right) \tag{6}$$

with the current i_{dm} through the demodulator. Given a high-voltage cable with a constant capacity C_l and an ohmic resistance R_l, the output voltage u_l can be written as

$$\frac{\mathrm{d}\,u_l}{\mathrm{d}\,t} = \frac{1}{C_l}\left(-\frac{u_l}{R_l} + i_{dm}\right). \tag{7}$$

As mentioned before, a simplified model of the demodulator is considered first. In this simplified model, the behavior of the thyristor is described by an ideal diode with negligible on-resistance and negligible threshold voltage $u_{th} = 0\,\mathrm{V}$. Under this assumption, the positive and negative branches of the demodulator are described by the adjustable resistors R_{dm}^{+} and R_{dm}^{-} and the current i_{dm} through the demodulator is given by

$$i_{dm} = \begin{cases} \dfrac{u_{dm}}{R_{dm}^{+}} & \text{if } u_{dm} \geq 0 \\ \dfrac{u_{dm}}{R_{dm}^{-}} & \text{if } u_{dm} < 0, \end{cases} \tag{8}$$

with the demodulator voltage $u_{dm} = u_r - u_l$ and $R_{dm}^{+}, R_{dm}^{-} \in [R_{on}, R_{off}]$. Equation (8) can be rewritten as

$$i_{dm} = \frac{1}{R_{off}}u_{dm} + \left(\frac{1}{R_{dm}^{+}} - \frac{1}{R_{off}}\right)g^{+} + \left(\frac{1}{R_{dm}^{-}} - \frac{1}{R_{off}}\right)g^{-} \tag{9}$$

with g^{+} and g^{-} defined by

$$g^{+} = \begin{cases} u_{dm} & \text{if } u_{dm} \geq 0 \\ 0 & \text{if } u_{dm} < 0 \end{cases} \tag{10}$$

and

$$g^{-} = u_{dm} - g^{+} \tag{11}$$

Remark 1 *For the simplest demodulation strategy, all thyristors of the positive branch are switched on for the positive half-wave and all thyristors of the negative branch for the negative half-wave of the desired output voltage u_l. Then the current i_{dm} through the demodulator during the positive half-wave is given by*

$$i_{dm} = \begin{cases} \dfrac{u_{dm}}{R_{on}} & \textit{if } u_{dm} \geq 0 \\ \dfrac{u_{dm}}{R_{off}} & \textit{if } u_{dm} < 0 \end{cases} \tag{12}$$

and by

$$i_{dm} = \begin{cases} \dfrac{u_{dm}}{R_{off}} & \textit{if } u_{dm} \geq 0 \\ \dfrac{u_{dm}}{R_{on}} & \textit{if } u_{dm} < 0 \end{cases} \tag{13}$$

during the negative half-wave. This simple demodulation strategy works well for small capacitive loads. For larger loads this yields, however, a significant deviation from the desired sinusoidal output voltage. Therefore, more advanced demodulation strategies which actively change the resistance R_{dm}^{+} and R_{dm}^{-} during charging and discharging of the capacitive load have to be utilized.

By defining the inductance matrix

$$\mathbf{L} = \begin{bmatrix} L_{\Sigma} & L_{ps1} & L_{ps2} \\ L_{ps1} & L_{p1} & 0 \\ L_{ps2} & 0 & L_{p2} \end{bmatrix} \tag{14}$$

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with $L_\Sigma = L_{s1} + L_{s2} + L_r$, the differential equations of the currents i_r, i_{p1} and i_{p2} according to (5), (1a) and (3a) can be rewritten in the form

$$\mathbf{L}\frac{\mathrm{d}}{\mathrm{d}\,t}\begin{bmatrix} i_r \\ i_{p1} \\ i_{p2} \end{bmatrix} = -\mathbf{R}\begin{bmatrix} i_r \\ i_{p1} \\ i_{p2} \end{bmatrix} + \begin{bmatrix} u_r \\ u_{p1} \\ u_{p2} \end{bmatrix}, \tag{15}$$

with $\mathbf{R} = \mathrm{diag}\left[R_\Sigma, R_{p1}, R_{p2}\right]$ and $R_\Sigma = R_{s1} + R_{s2} + R_r$. As previously mentioned, the primary voltages u_{p1} and u_{p2} of the exciter coils are generated by the two full bridges in the power module. They have a pulse-width-modulated rectangular shape, as illustrated in Fig. 4 with a fixed amplitude u_p and adjustable duty cycles χ_1 and χ_2, which can be varied in the range of $0 \leq \chi_1, \chi_2 \leq 1$. The desired amplitude modulation of the resonant voltage u_r is achieved by the choice of the cycle times T_{p1} and T_{p2} of the power module voltages according to

$$T_{p1} = \frac{2\pi}{\omega_{p1}} = \frac{2\pi}{\omega_r - \omega_\Delta} \tag{16a}$$

$$T_{p2} = \frac{2\pi}{\omega_{p2}} = \frac{2\pi}{\omega_r + \omega_\Delta}. \tag{16b}$$

The mathematical description of the power module voltages u_{p1} and u_{p2} is then given by

$$u_{p1} = \begin{cases} u_p & \text{if } 0 < t \leq \chi_1 \frac{T_{p1}}{2} \\ 0 & \text{if } \chi_1 \frac{T_{p1}}{2} < t \leq \frac{T_{p1}}{2} \\ -u_p & \text{if } \frac{T_{p1}}{2} < t \leq \frac{T_{p1}}{2} + \chi_1 \frac{T_{p1}}{2} \\ 0 & \text{if } \frac{T_{p1}}{2} + \chi_1 \frac{T_{p1}}{2} < t \leq T_{p1} \end{cases} \tag{17a}$$

$$u_{p2} = \begin{cases} u_p & \text{if } 0 < t \leq \chi_2 \frac{T_{p2}}{2} \\ 0 & \text{if } \chi_2 \frac{T_{p2}}{2} < t \leq \frac{T_{p2}}{2} \\ -u_p & \text{if } \frac{T_{p2}}{2} < t \leq \frac{T_{p2}}{2} + \chi_2 \frac{T_{p2}}{2} \\ 0 & \text{if } \frac{T_{p2}}{2} + \chi_2 \frac{T_{p2}}{2} < t \leq T_{p2}. \end{cases} \tag{17b}$$

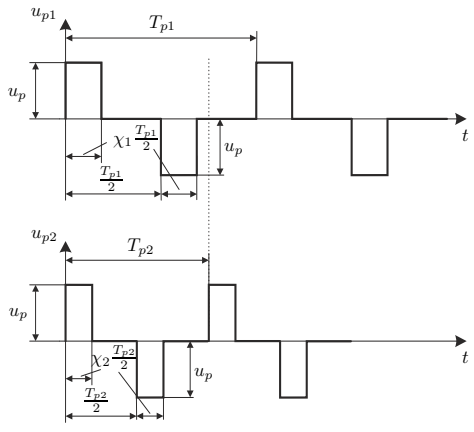

Fig. 4. Power module output voltages u_{p1} and u_{p2}.

Based on the basic mathematical model, a first simulation study is given to illustrate the functional principle of the

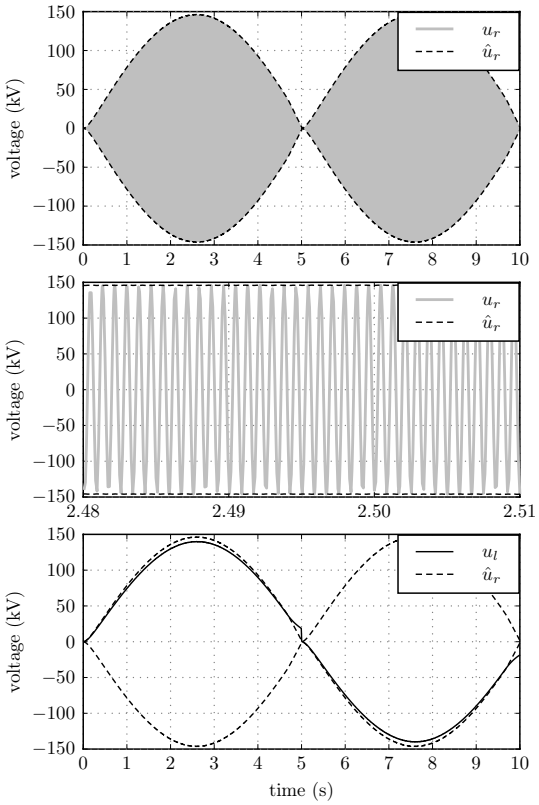

Fig. 5. Simulation results for $R_l = 300\,\mathrm{M\Omega}$, $C_l = 50\,\mathrm{nF}$ and $\chi_1 = \chi_2 = 0.15$.

DRT test system. For this, the mathematical model was implemented in MATLAB/SIMULINK and parametrized with the nominal values of the DRT prototype. The simulation was performed with a resistive-capacitive load of $R_l = 300\,\mathrm{M\Omega}$, $C_l = 50\,\mathrm{nF}$ and the duty cycles $\chi_1 = \chi_2 = 0.15$. The value of the resistive part of the load is mainly determined by the value of an internal resistor divider, which is used for the measurement of the output voltage u_l, see Fig. 10(b). The resonant angular frequency, which is determined by the nominal values of the resonant capacitance and inductance is given by $\omega_r = 2\pi 1203\,\mathrm{rad\,s^{-1}}$ and the angular frequency of the output voltage u_l was chosen as $\omega_\Delta = 2\pi 0.1\,\mathrm{rad\,s^{-1}}$.

The choice of this small load capacity makes it possible to apply the simplest demodulation strategy as proposed in Remark 1. Fig. 5 depicts both the signals and the corresponding envelope of the signals, henceforth referred to by the $\hat{(\cdot)}$ symbol. As can be seen, the simple demodulation strategy already leads to a nearly perfect demodulation of the amplitude modulated high-voltage signal u_r. Only near the zero crossings, a slight deviation from the desired sinusoidal output voltage u_l is apparent. This deviation could be avoided by actively reducing the value of the discharge resistor R_d. This reduction requires the use of a more complex demodulation strategy, i.e. a suitable switching of the thyristors in the SVU. The amplitude $\hat{u}_l$ of the output voltage u_l is smaller than the amplitude $\hat{u}_r$ of the resonator voltage, which is due to the

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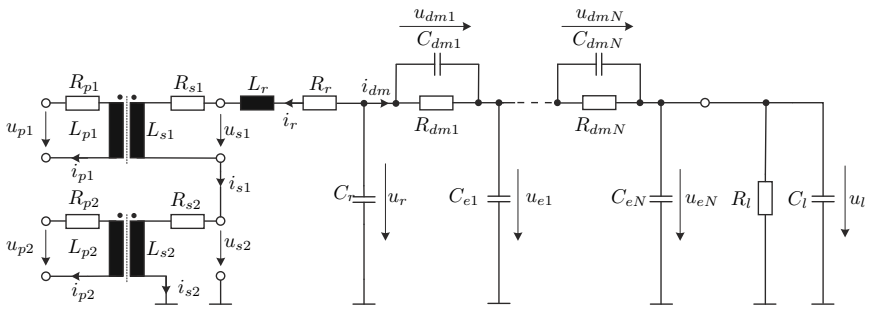

Fig. 6. Circuit diagram of the extended model with discrete demodulator modules.

losses in the SVU.

B. Analysis of the influence of stray capacitances

The components of the high-voltage part (except for the power module) are installed in a container filled with insulating oil. Stray capacitances do exist between the housing of the container and the modules of the demodulator. These capacitances are modeled by means of $C_{en}, n = 1, \ldots, N$ according to Fig. 6.

As already indicated in Section II, in particular Fig. 2, capacitances $C_{dmn}, n = 1, \ldots, N$ are connected in parallel to the SVU boards of each module in order to ensure an equal voltage drop for all boards and modules, respectively.

Thus, the system equations of the N demodulator modules, see Fig. 6, read as

$$\mathbf{C}\begin{bmatrix} \dot{u}_r \\ \dot{u}_{dm1} \\ \dot{u}_{dm2} \\ \vdots \\ \dot{u}_{dmN} \end{bmatrix} = \begin{bmatrix} -i_r - i_{R_{dm1}} \\ -i_{R_{dm1}} + i_{R_{dm2}} \\ -i_{R_{dm2}} + i_{R_{dm3}} \\ \vdots \\ \frac{u_r}{R_l} - \frac{u_{dm1}}{R_l} - \ldots - \frac{u_{dmN}}{R_l} - i_{R_{dmN}} \end{bmatrix} \tag{18}$$

with the voltage drop u_{dmn} along the n-th module and $i_{R_{dmn}}$ denoting the current through the corresponding resistive part. The matrix $\mathbf{C}$ consists of all capacitances of the test system and is given in (19) with $C_l^* = C_l + C_{eN}$. The currents $i_{R_{dmn}}$ are calculated by

$$i_{R_{dmn}} = \frac{1}{R_{offn}} u_{dmn} + \left(\frac{1}{R_{dmn}^+} - \frac{1}{R_{offn}}\right) g_n^+ + \left(\frac{1}{R_{dmn}^-} - \frac{1}{R_{offn}}\right) g_n^-, \tag{20}$$

where R_{dmn}^+, $R_{dmn}^- \in \{R_{onn}, R_{offn}\}$ describe the effective resistance of the positive and negative thyristor branch of the n-th demodulator module. The terms g_n^+ and g_n^- are defined in the same way as in (10) and (11) for $n = 1, \ldots, N$. The mathematical model of the complete DRT test system of Fig. 6 is given by (18) in combination with the equations of the resonator (15) and the power module voltages u_{p1} and u_{p2} according to (17).

The values of the stray capacitances $C_{en}, n = 1, \ldots, N$ were estimated by means of the field simulation software ELECTRO 2D/RS in combination with the mathematical model given by (18). As a result, for the modules placed close to the housing walls, i.e. modules 1 to 5 and 16 to 20, a value of 70 pF and for all other modules a value of 50 pF was estimated. Fig. 7 shows the measured and simulated voltage distribution over the $N = 20$ demodulator modules of the DRT prototype. Thereby, the demodulator was deactivated, i.e. $R_{dm}^+ = R_{dm}^- = R_{off}$, a resonant voltage $\hat{u}_r$ of 30 kV was chosen and all capacitances $C_{dmn}, n = 1, \ldots, N$ were set to the nominal value of 88 pF. It can be seen that the voltage drop per module is significantly higher for the first 5 modules compared to the remaining 15 modules. At this point it is worth noting that the electric field strength of the individual modules is limited. Thus, this inhomogeneous voltage distribution reduces the maximum output voltage of the DRT system. Clearly, a completely equal distribution of the voltage drops in the form $u_{dmn} = \frac{u_{dm}}{N}$, $n = 1, \ldots, N$ would be preferable, see the dashed line in Fig. 7. A closer

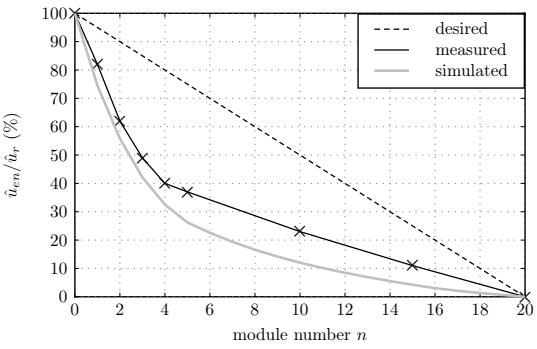

Fig. 7. Influence of the stray capacitances on the voltage distribution of the SVU modules for nominal capacitances $C_{dmn} = 88$ pF.

look at the circuit diagram of Fig. 6 reveals that the stray capacitances C_{e1} to C_{eN} together with the capacitances C_{dm1} to C_{dmN} form a capacitive voltage divider, which is the reason for the inhomogeneous voltage distribution. Thus, an obvious approach to improve the homogeneity is to significantly increase the values of the SVU capacitances C_{dmn}. Fig. 8 shows the results for C_{dmn} =8.8 nF, an increase of a factor 100. As can be seen, both from the measurement and simulation results, the first modules are still loaded with higher voltages such that a further increase of C_{dmn} for $n = 1, \ldots, 5$ seems to be reasonable. The simulation results for C_{dmn} =17.6 nF,

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$$\mathbf{C} = \begin{bmatrix} C_r & C_{dm1} & 0 & 0 & 0 & \cdots & 0 & 0 \\ -C_{e1} & (C_{dm1}+C_{e1}) & -C_{dm2} & 0 & 0 & \cdots & 0 & 0 \\ -C_{e2} & C_{e2} & (C_{dm2}+C_{e2}) & -C_{dm3} & 0 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ -C_l^* & C_l^* & C_l^* & C_l^* & C_l^* & \cdots & C_l^* & (C_l^*+C_{dmN}) \end{bmatrix} \tag{19}$$

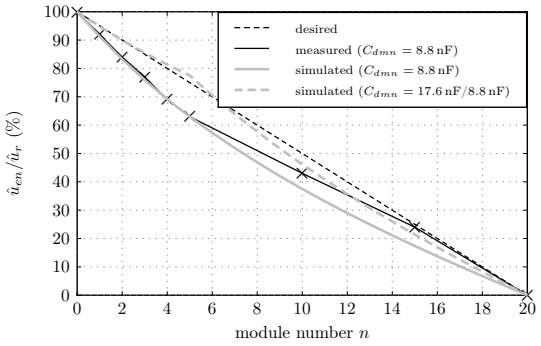

Fig. 8. Influence of the SVU capacitances on the voltage distribution of the SVU modules with adjusted values of C_{dmn}.

$n = 1, \ldots, 5$ and C_{dmn} =8.8 nF, $n = 6, \ldots, 20$ given in Fig. 8 confirm that the desired homogeneous voltage distribution can be achieved with this measure.

C. Analysis of the non-idealities of the demodulator modules

Up to now the SVU modules have been considered in an idealized form, assuming an adjustable resistance to represent the system behavior. In reality, the adjustable resistance is realized by means of high-voltage thyristors which have to be adequately switched on and off. Naturally, a thyristor exhibits a nonlinear behavior. Moreover, an energy recovery circuit is necessary in order to provide the energy which is needed to actively switch the thyristors. Therefore, this section is concerned with the analysis, the quantification, and the modeling of these non-idealities.

The on-state slope resistance of the high-voltage thyristors is approximately 12 mΩ, which is negligible compared to the loading resistor R_{lo} (connected in series) with a value of 50 Ω. The second non-ideality of the thyristors is the threshold voltage whose influence can be easily taken into account in the calculation of g_n^+ and g_n^- (see (10) and (11)) by increasing the threshold from 0V to 25V.

The most significant influence on the system behavior is due to the energy recovery circuit. This circuit consists of a high-voltage transformer with a switching regulator, which charges a super cap storage capacitor. The super cap is used to ensure a constant supply voltage to the switching circuit of the thyristors. The amount of energy drawn from the high-voltage is a function of the voltage u_{dmn} of the considered SVU board and the state of charge of the storage capacity. The recovery circuit was designed in such a way that the energy consumption for constant state of charge of the storage capacitor is nearly constant over the whole operating range of the voltage, i.e. smaller voltages cause higher currents into the recovery circuit.

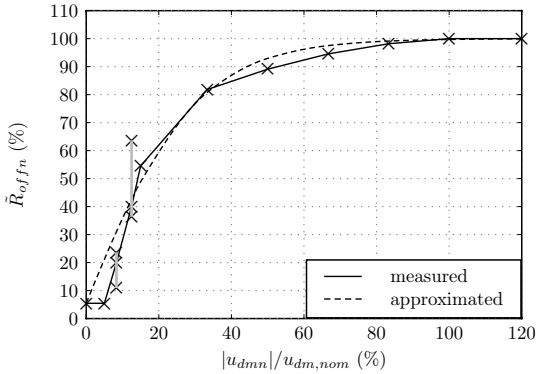

Fig. 9. Effective discharge resistor during active SVU switching - measurement and approximation.

Measurements of the current into the recovery circuit show that the recovery circuit's influence can be approximated by an equivalent discharge resistor $\tilde{R}_{offn}$, which is a function of the voltage u_{dmn} applied to the module n. The results of these measurements are depicted as crosses in Fig. 9. An exact modeling of the behavior of the recovery circuit is difficult and not useful for the modeling of the DRT test system, since the variation due to the state of charge of the storage capacity (grey lines in Fig. 9) is generally unknown during normal operation. Thus, a simplified mathematical description of the main influence of the recovery circuit is given in the form

$$\tilde{R}_{offn}(u_{dmn}) = R_{offn} \tanh\left(a_0\left(\frac{|u_{dmn}|}{u_{dm,nom}} + a_1\right)\right). \tag{21}$$

The model parameters a_0 and a_1 are calculated by a nonlinear least squares fit of the measurement data. Fig. 9 depicts a comparison of the measurements with the approximation (21). The current $i_{R_{dmn}}$ through an SVU module can thus be described by means of (20) with R_{offn} replaced by $\tilde{R}_{offn}(u_{dmn})$ according to (21).

IV. Measurement and Simulation Results

In order to validate the developed mathematical model, several measurements were performed on a DRT prototype designed for voltages up to 200 kV rms and maximum loads of 0.75 µF. The measurements were accomplished at Mohaupt High Voltage facility in Mieders, Austria, with a measurement set-up shown in Fig. 10(a). Fig. 10(b) depicts the circuit diagram of the complete measurement set-up. In this set-up, the output voltage u_l, the resonator voltage u_r, the primary voltage u_{p1}, both primary currents i_{p1} and i_{p2} and the resonator current i_r can be measured. Moreover, the intermediate

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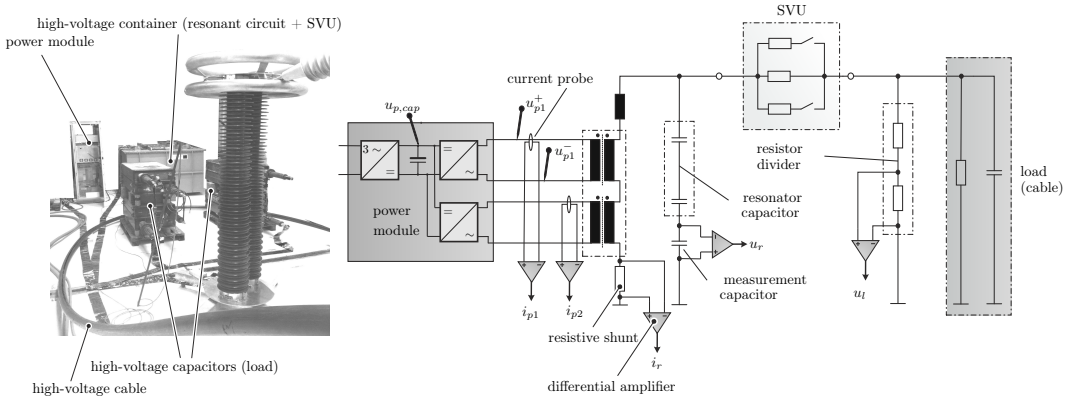

(a) Measurement set-up at Mohaupt High Voltage facility.

(b) DRT circuit diagram including the measurement set-up.

Fig. 10. Measurement set-up for the model validation of the DRT prototype.

DC voltage $u_{p,cap}$ of the power module is available. In order to suppress disturbances caused e.g. by the switching of the power module, all measurements were performed by means of differential amplifiers. The measured signals were recorded using a DSPACE real-time system at a sampling rate of 20 kS/s. To ensure a sufficient time resolution, the primary voltage u_{p1} was recorded with a Tectronix oscilloscope at a sampling rate of 2.5 GS/s.

The parametrization of the demodulator and its capacity network comprising the stray and parallel capacitances has already been shown in Section III-B. Thus, this section is primarily concerned with the validation of the mathematical model of the power module and the resonant circuit, using a deactivated SVU. Furthermore, measurements with a very small capacitive load and activated SVU are accomplished to allow a first comparison of the functional principle of the DRT system with the mathematical model.

The first measurement deals with the validation of the shape and pulse width of the power module voltages. Three high-voltage probes were used to measure the voltages $u_{p,cap}$, u_{p1}^- and u_{p1}^+ as shown in Fig. 10(b). The set-up allows a potential-free measurement of the voltage $u_{p1}^+ - u_{p1}^-$. Since the power module is symmetric, the measurement was only performed for the output voltage u_{p1}. The upper part of Fig. 11 depicts the measured voltages for the duty cycles $\chi_1 = \chi_2 = 0.166$. It can be seen that the intermediate voltage $u_{p,cap}$ is moving with respect to ground, which is of course directly mapped to the output voltages u_{p1}^+ and u_{p1}^-. The difference $u_{p1} = u_{p1}^+ - u_{p1}^-$ shown in the lower part of Fig. 11, however, exhibits a constant amplitude of approximately 540 V, as it is presumed for the mathematical model.

Next the model of the resonant circuit with the power module but without the SVU is validated. In order to do so, the SVU-modules were detached and the two power module currents i_{p1} and i_{p2}, the resonant current i_r and the voltage across the resonant capacitor u_r were measured for different duty cycles of the power module voltages u_{p1} and

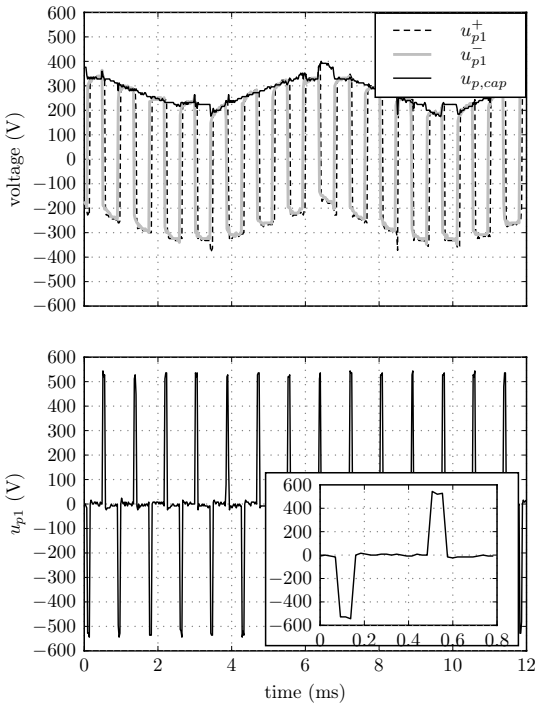

Fig. 11. Measured power module voltage u_{p1} over several periods.

u_{p2}. The envelopes of the measured and simulated signals are depicted in Fig. 12 and 13 for two different duty cycles $\chi = 0.074$ and $\chi = 0.166$ and a resonant angular frequency of $\omega_r = 2\pi 1200\,\mathrm{rad\,s^{-1}}$. As can be seen, a good agreement is achieved by the mathematical model, in particular for the envelope of the resonant voltage u_r. The input currents i_{p1} and i_{p2} are also quite well reproduced by the mathematical model. A closer look at the measurement results shows that the two exciter transformers are not completely symmetric,

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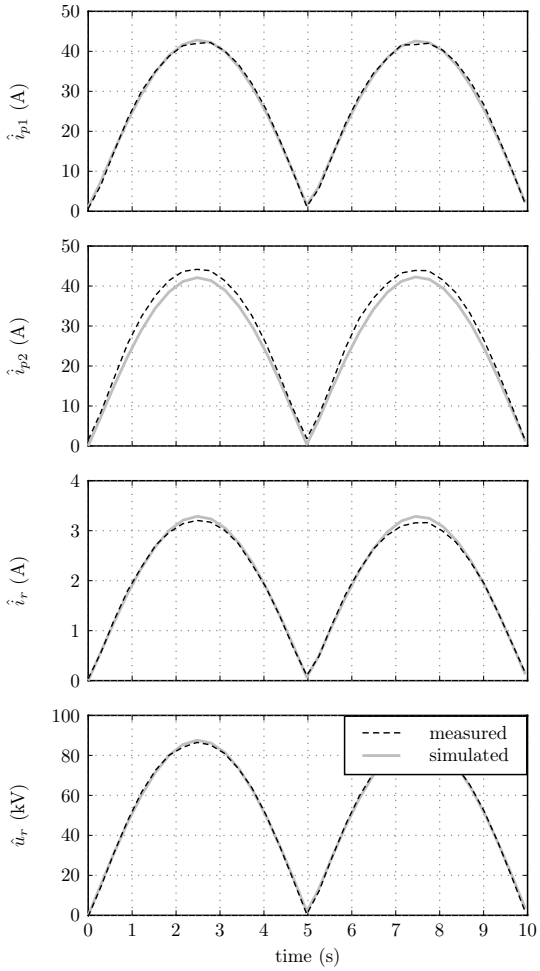

Fig. 12. Comparison of the measurements with the simulation results for $\chi_1 = \chi_2 = 0.074$.

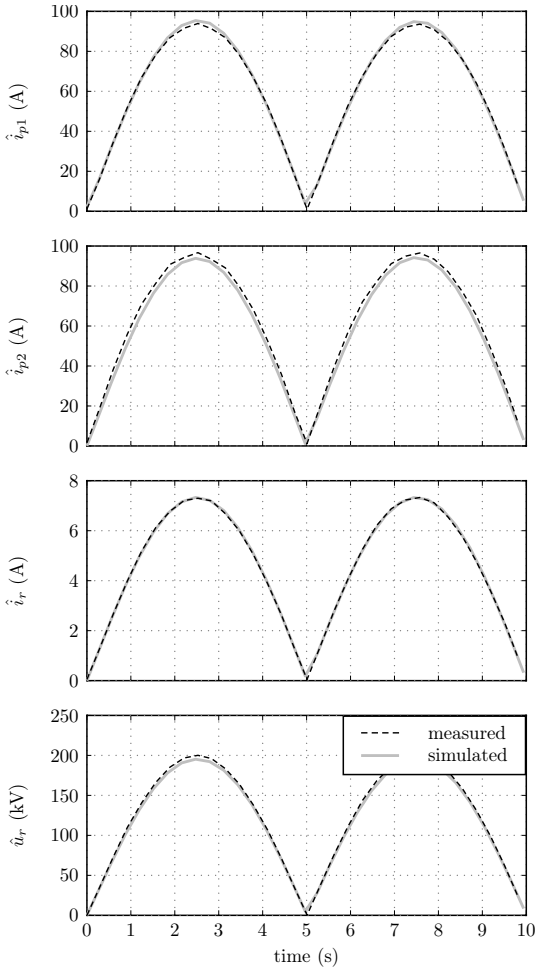

Fig. 13. Comparison of the measurements with the simulation results for $\chi_1 = \chi_2 = 0.166$.

which is directly reflected in the slightly higher amplitude of the measured current i_{p2}.

In the next measurements the overall system with a resistive-capacitive load of $R_l = 300\,\mathrm{M\Omega}$ and $C_l = 7.5\,\mathrm{nF}$ are considered, see Fig. 14. The measurements were performed at power module duty cycles $\chi_1 = \chi_2 = 0.148$, a resonant angular frequency of $\omega_r = 2\pi 1100\,\mathrm{rad\,s^{-1}}$ and an output angular frequency of $\omega_\Delta = 2\pi 0.097\,\mathrm{rad\,s^{-1}}$. Note that the change in the resonant angular frequency is due to the additional capacitances of the SVU-modules, which are now attached to the resonant circuit.

Comparing the measurements of the voltages u_r and u_l with the simulation results shows that the behavior of the DRT system is very well captured by the mathematical model. Due to disturbances in the current measurements there is a deviation between the measured and simulated input currents i_{p1} and i_{p2}. The measurements were performed at fully charged super capacitors. Thus, the influence of the energy recovery circuit on the system behavior was negligibly small, and (21) with adjusted model parameters was used in the simulations.

Now, a comparison of the model with the measurements for increased loads would be interesting. Using a load capacity of 400 nF together with the basic demodulation strategy in simulation leads to a resonant voltage $\hat{u}_r$ and a load voltage u_l as depicted in Fig. 15. As can be seen, the shape of the resulting load voltage is far from being sinusoidal and exhibits a high residual voltage when switching from the positive to the negative half-wave. In the real system, switching at these high-voltages would lead to a damage of the DRT system. Thus, it is not possible to validate the model for larger loads at this stage. As already outlined before, an advanced demodulation strategy is necessary in order to handle larger loads.

However, based on the results of the model validation presented in this paper, the authors are confident that the model is also accurate for larger loads and can therefore be used as a solid basis for the controller design and the development of advanced demodulation concepts.

V. System Analysis

In the mathematical modeling of the last sections, basically two effects were identified that lead to a deviation of the real

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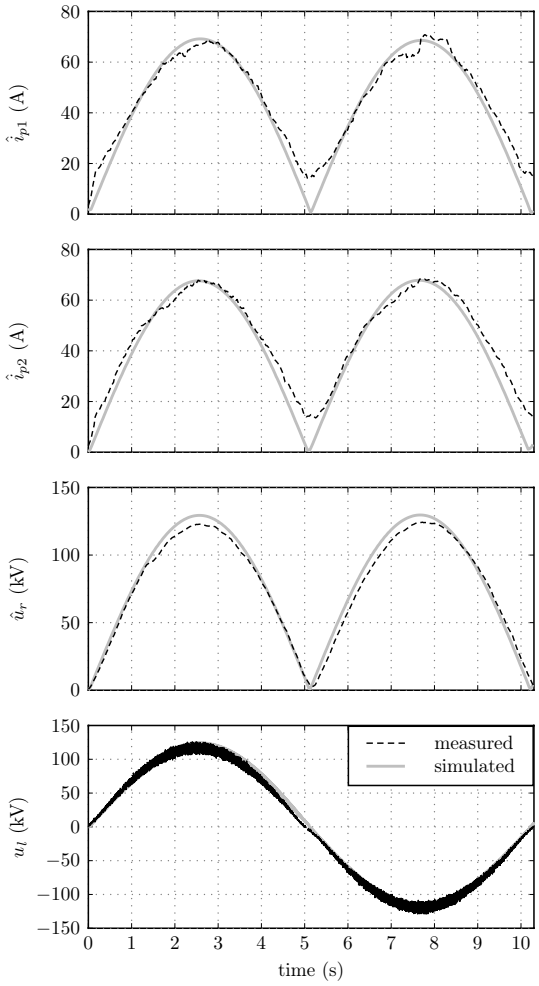

Fig. 14. Comparison of the measurements with the simulation results for a small capacitive load of $C_l = 7.5\,\text{nF}$ and $\chi_1 = \chi_2 = 0.148$.

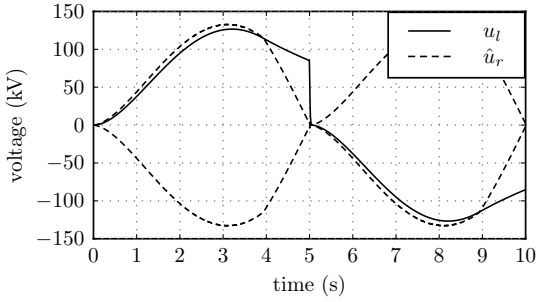

Fig. 15. Simulation results for $C_l = 400\,\text{nF}$ and $\chi_1 = \chi_2 = 0.15$.

system behavior from the ideal one, i.e. the stray capacitances to earth and the energy recovery system. In addition, the load capacity C_l, i.e. the capacity of the cable to be tested, is not exactly known. This section analyzes the effects of these non-idealities by means of simulations of the mathematical model.

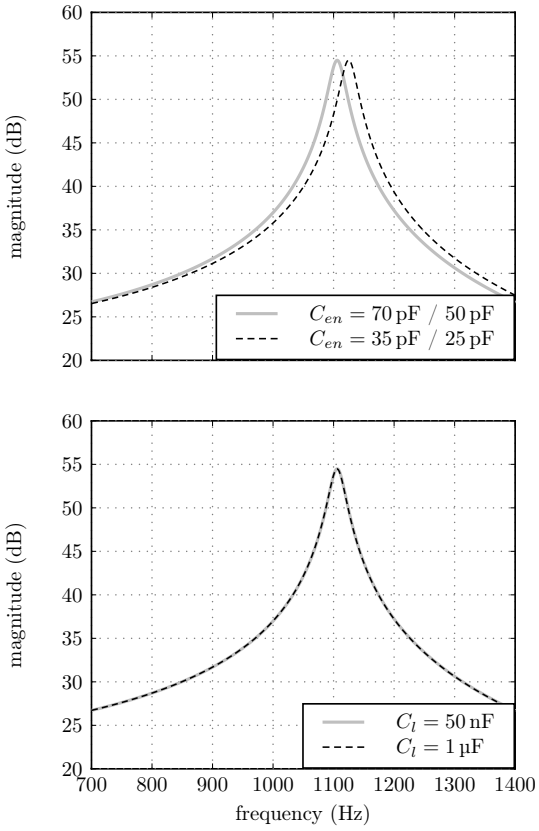

Fig. 16. Resonant frequency depending on the cable capacity and the SVU capacitances.

A. *Influence of stray and load capacitances*

The essential idea of the high-voltage test system is to excite the series resonant circuit at its resonant frequency. Due to the high quality factor, the exact knowledge of the resonant frequency is inevitable for an optimal operation of the DRT test system.

The resonant frequency is defined by the capacitances and the resonant inductance in the DRT test system. Considering constant values of the resonant capacity and inductance, the resonant frequency can only change due to varying values of the cable capacity or stray capacitances. As already mentioned, the exact capacity of the test cable is generally unknown. Furthermore, the values of the stray capacitances vary depending on the system set-up. For this reason, this subsection deals with the quantification of the influence of these capacitances on the resonant frequency.

Deactivating the SVU, i.e. setting $R^+_{dmn} = R^-_{dmn} = R_{offn}$, leads to a linear mathematical model of the DRT test system. The system's frequency response can then be analyzed by means of the transfer function from the input u_{p1} (the transfer function of u_{p2} is equal) to the output u_r. The frequency response of the resulting transfer function for nominal parameters of the SVU capacitors, i.e. $C_{dmn} = 17.9\,\text{nF}$, $n = 1, \ldots, 5$, $C_{dmn} = 8.8\,\text{nF}$, $n = 6, \ldots, 20$, $C_{en} = 70\,\text{pF}$, $n = 1, \ldots, 5$ and $n = 16, \ldots, 20$, $C_{en} = 50\,\text{pF}$, $n = 6, \ldots, 15$, is depicted

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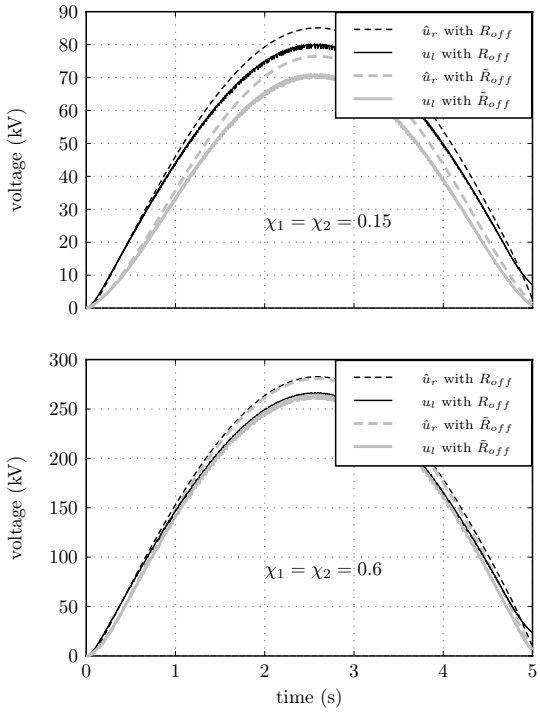

Fig. 17. Influence of the energy recovery circuit on the system's behavior, demonstrated for different voltage levels.

in Fig. 16. Since the exact value of the stray capacitances is difficult to obtain, a comparison of the transfer function for halved values of the stray capacitances is given in Fig. 16. It can be seen that the resonant frequency is slightly increased from 1106 Hz to 1125 Hz. In contrast to this, a variation of the load capacity from $C_l = 50\,\text{nF}$ to $C_l = 1\,\mu\text{F}$ does not measurably change the resonant frequency, see the lower part of Fig. 16.

This result brings along the big advantage that the resonant frequency of the DRT test system only has to be identified once after assembling the system and can be kept constant for different cable tests.

B. Influence of the energy recovery circuit

As described in Section III-C, the energy recovery circuit changes the effective value of the discharge resistors. In order to demonstrate the influence of the energy recovery circuit on the system's behavior, two different simulation scenarios will be considered.

The ideal system neglecting the energy recovery system is compared with a realistic model of the SVU including (21). The simulations, depicted in Fig. 17, were executed with a small capacitive load of $C_l = 50\,\text{nF}$ and two different duty cycles of $\chi_1 = \chi_2 = 0.15$ and $\chi_1 = \chi_2 = 0.6$. As can be seen in the upper part of Fig. 17, there is a significant reduction in the amplitudes of the resonant voltage u_r and the output voltage u_l in the case of small duty cycles if the energy recovery circuit is considered ($\hat{u}_r$ and u_l with $\tilde{R}_{off}$). In this case, the voltage across each demodulator module is approximately 25 % of its nominal value, which leads to a significant decrease in the value of the equivalent discharge resistor of each SVU module, see Fig. 9. This small discharge resistors cause a larger load to the series resonant circuit, which directly results in the smaller amplitudes depicted in the upper part of Fig. 17. Having a look at the lower part of Fig. 17 shows that this effect gets, as it is expected, smaller for increasing values of χ_1 and χ_2. This is, of course, due to the fact that $\tilde{R}_{off}$ tends to R_{off} for large values of u_{dm}. Thus, this effect has to be taken into account in the derivation of a control strategy.

VI. Conclusion

In this contribution, a new type of VLF high-voltage test system for the on-site testing of high-voltage cables was presented. A detailed mathematical model of the test system was proposed, which was used to analyze and design several system parts. The model was validated and parametrized by means of different measurements performed on a prototype designed for 200 kV rms and maximum loads of 0.75 µF. In simulation studies it could be shown that for the testing of longer high-voltage cables, i.e. large capacitive loads, a suitable control strategy is needed. For this reason, the mathematical model will be used in future works to develop control strategies, minimizing the power losses and optimizing the THD (Total Harmonic Distortion) value of the desired test voltage. Furthermore, mathematical optimization techniques will be applied to the model to calculate different distributions of the values of the SVU resistors and analyze their influence on the system's behavior.

Acknowledgment

A main part of the research for this paper has been sponsored by the FFG-Austrian Research Promotion Agency in the BRIDGE-project no. 829582. Further thanks goes to Peter Mohaupt and the employees of Mohaupt High Voltage GmbH for supporting the measurement campaigns.

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