Controller design and experimental validation of a very low frequency high-voltage test system

authored by **W. Kemmetmüller, S. Eberharter, and A. Kugi**

and published in *Control Engineering Practice*.

Cite this article as:

W. Kemmetmüller, S. Eberharter, and A. Kugi, "Controller design and experimental validation of a very low frequency high-voltage test system", *Control Engineering Practice*, vol. 37, pp. 32–42, Apr. 2015. DOI: 10.1016/j.conengprac.2014.12.011

BibTex entry:

```
@ARTICLE{kemmetmueller_2015,
  author = {W. Kemmetm\"uller and S. Eberharter and A. Kugi},
  title = {Controller design and experimental validation of a very low frequency
       high-voltage test system},
  journal = {Control Engineering Practice},
  year = {2015},
  volume = {37},
  pages = {32-42},
  month = {April},
  doi = {10.1016/j.conengprac.2014.12.011},
  url = {http://www.sciencedirect.com/science/article/pii/S0967066114002846}
}
```

Link to original paper:

http://dx.doi.org/10.1016/j.conengprac.2014.12.011
http://www.sciencedirect.com/science/article/pii/S0967066114002846

Contact:

Automation and Control Institute (ACIN)
Vienna University of Technology
Gusshausstrasse 27-29/E376
1040 Vienna, Austria

Internet: www.acin.tuwien.ac.at
E-mail: office@acin.tuwien.ac.at
Phone: +43 1 58801 37601
Fax: +43 1 58801 37699

Controller design and experimental validation of a very low frequency high-voltage test system

W. Kemmetmüller[a,*], S. Eberharter[a], A. Kugi[a]

[a] *Automation and Control Institute, Vienna University of Technology, Gusshausstr. 27 - 29, 1040 Vienna, Austria*

Abstract

This paper presents the design of a quasi optimal controller for a new type of very low frequency (VLF) high-voltage test system for on-site cable tests. The test system is based on the Differential Resonance Technology (DRT), which allows a light weight and compact construction. The high requirements regarding quality and accuracy of VLF test voltages can only be achieved with a suitable control concept. In this work, a two degrees-of-freedom control strategy comprising a feedforward and a feedback control in combination with an estimator for the unknown cable capacitance is proposed. The controller design is based on an envelope model which describes the (nonlinear) envelope dynamics of the occurring amplitude modulated signals. The feasibility of the proposed control strategy is verified by a number of measurements on a prototype system for cable tests up to 200 kV rms. The measurement results show that the generated test voltage has a total harmonic distortion (THD) of less than 0.1 %, which is significantly better than the requirements of sinusoidal VLF test voltages. Moreover, the control strategy has the ability to cover a wide range of cable capacitances, desired amplitudes of the output voltage and desired test frequencies.

Keywords: high-voltage, cable testing, on-site testing, very low frequency, envelope model, feedback control

1. Introduction

Failures in energy supply networks are always associated with very high costs, such as failure repair costs or costs caused by long down times. To avoid these costs, a fail-safe operation of energy supply networks is getting more and more important. Therefore, high- and ultra-high-voltage cables, used for the energy distribution in these networks, have to pass strict quality tests. They are not only checked in factory acceptance tests after their production, but are also examined in on-site tests when they are already installed. For these on-site tests, the test systems have to feature a compact and lightweight design.

In view of these demands, a new type of cable test method with very low frequencies (VLF) in the range of 0.01 Hz to 0.1 Hz was established, reducing the amount of reactive power and, thus, the size and weight of the test device, see Putter et al. (2012); IEEE Power Engineering Society (2004); Pietsch and Hausschild (2005); Krüger et al. (1990); Muhr et al. (2001); Coors and Schierig (2008). For VLF tests of mid- and high-voltage cables up to 80 kV rms, several test systems are already available Baur Prüf- und Messtechnik GmbH (2006); R. Reid (1999); Stanley G. Peschel (2001); Neumann Elektrotechnik GmbH (2004); Seesanga et al. (2008). To extend the range of VLF test systems to higher voltage levels, a VLF test system based on the so called Differential Resonance Technology (DRT) was developed. This type of VLF system allows a mobile VLF testing of cables up to 500 kV rms and higher, see Eberharter et al. (2014); Mohaupt and Bergmann (2010).

In the design of VLF cable test systems, several challenges have to be faced with. First, high standards are imposed on the quality and accuracy of the test voltage. For example, the total harmonic distortion (THD) of a sinusoidal VLF test voltage has to be less than 5 percent, see IEC 60060-1 and IEC 60060-3. Second, the cable test system has to provide a test voltage of constant quality for the whole operation range of high-voltage cables. Maintaining a constant quality test voltage is a challenging task as the characteristics of high-voltage cables strongly vary with their length and structure. E.g., the cable capacitance may take values from a few nF up to several µF. Finally, the power consumption of the test system has to be minimized to allow for an energy efficient operation. In order to meet all these requirements, a suitable control of the test system is indispensable. An appropriate control strategy for a VLF cable test system with sinusoidal test voltages up to 80 kV rms can be found in Chao et al. (2009, 2010). However, this control strategy is designed for a particular VLF test system, which uses high-voltage multipliers and DC sources for the generation of the VLF test voltage and, therefore, cannot be applied to the DRT system under consideration.

For this reason, the present paper deals with the design

* *Corresponding author:* Tel./Fax:+43(0)1 58801-376261/-37699
Email addresses: kemmetmueller@acin.tuwien.ac.at (W. Kemmetmüller), eberharter@acin.tuwien.ac.at (S. Eberharter), kugi@acin.tuwien.ac.at (A. Kugi)

Post-print version of the article: W. Kemmetmüller, S. Eberharter, and A. Kugi, "Controller design and experimental validation of a very low frequency high-voltage test system", *Control Engineering Practice*, vol. 37, pp. 32–42, Apr. 2015. DOI: 10.1016/j.conengprac.2014.12.011
The content of this post-print version is identical to the published paper but without the publisher's final layout or copy editing.

and experimental validation of a two degrees-of-freedom control strategy for the new DRT test system. The control strategy consists of a feedforward and a feedback control of the amplitude and shape of the VLF test voltage. It is based on a detailed analysis of the DRT system and the results of a static optimization problem as presented in Kemmetmüller et al. (2014). The control strategy is derived from an envelope model of the DRT test system, which is shortly summarized in Section 2. Section 3 focuses on the design of the feedforward and feedback part of the controller. Since the exact capacitance of the high-voltage cable is normally unknown before the testing, the control strategy is extended by an estimation algorithm for the identification of this parameter. The estimation of the cable capacitance is accomplished by a least squares approach in Section 4. In Section 5, the control strategy and the estimation algorithm are validated in simulations. Section 6 describes the real-time implementation of the control concept on the prototyping hardware and presents measurement results. The last section, Section 7, contains some conclusions.

2. Mathematical Modeling

This section summarizes the mathematical model of the DRT system, which is the basis for the controller design. First, a short description of the functional principle of the DRT system is given. Afterwards, a simplified mathematical model and an envelope model are derived. For a more detailed system description and modeling of the DRT system, the reader is referred to Eberharter et al. (2014).

2.1. System description

A schematic of the functional principle of the DRT system is depicted in Figure 1. One of the main components of the system is the resonant circuit, which is excited at its resonance by the input voltages u_{p1} and u_{p2}. The voltages are generated by two full-bridges in the power module and have a pulse width modulated rectangular shape with a fixed amplitude u_p and adjustable pulse widths $\chi_1 = \chi_2 = \chi$, which can be varied in the range $0 \leq \chi \leq 1$.

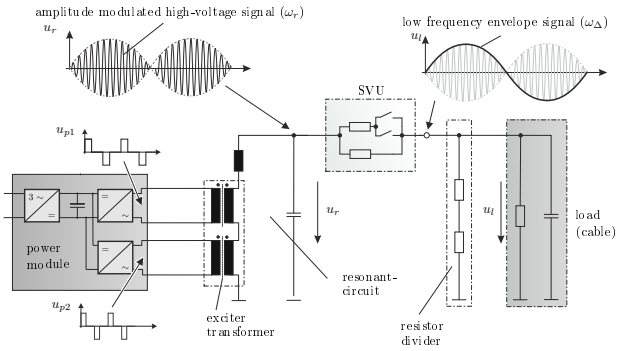

Figure 1: Schematic of the DRT test system.

By an adequate change of χ, the voltage u_r at the resonant capacitor results in an amplitude modulated high-voltage signal, comprising the carrier angular frequency ω_r and the desired very low angular frequency ω_Δ of the output test voltage u_l.

The output voltage u_l is then generated by a suitable switching of the thyristors in the demodulator (SVU - switched valve unit). Figure 2 shows a simplified circuit

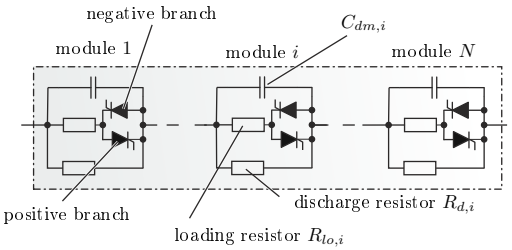

Figure 2: Simplified circuit diagram of the demodulator.

diagram of the demodulator which consits of N discrete modules. Each module is composed of a high-voltage thyristor for the positive and negative branch connected in series with a loading resistor $R_{lo,i}$. In parallel to this arrangement, a discharging resistor $R_{d,i}$ and a capacity $C_{dm,i}$, which is required to guarantee a homogeneous voltage distribution across the modules Eberharter et al. (2014), are placed. The energy required for the switching of the thyristors is extracted from the high carrier frequency voltage across each SVU module, see Eberharter et al. (2014).

2.2. Model equations

Figure 3 shows an equivalent circuit diagram of the DRT system presented in Section 2.1. For the development of

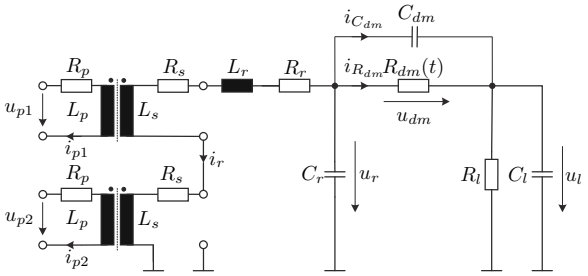

Figure 3: Equivalent circuit diagram of the DRT system with a continuously adjustable demodulator resistor $R_{dm}(t)$ and a capacitance C_{dm} in parallel.

the mathematical model, the following assumptions and simplifications are made, see also Eberharter et al. (2014); Kemmetmüller et al. (2014): The overall demodulator can be approximated by a continuously adjustable resistor $R_{dm}(t)$ and a parallel capacitance C_{dm}, neglecting the modular design of the demodulator. The value of C_{dm}

Post-print version of the article: W. Kemmetmüller, S. Eberharter, and A. Kugi, "Controller design and experimental validation of a very low frequency high-voltage test system", *Control Engineering Practice*, vol. 37, pp. 32–42, Apr. 2015. DOI: 10.1016/j.conengprac.2014.12.011
The content of this post-print version is identical to the published paper but without the publisher's final layout or copy editing.

is defined by a capacitance network comprising the parallel capacitances $C_{dm,i}$ of the N SVU modules and the stray capacitances between the modules and the housing of the DRT system. By means of a defined switching sequence of the thyristors, the value of $R_{dm}(t)$ can be varied between R_{on} and R_{off} with $R_{on} = \sum_{i=1}^{N} R_{lo,i}$ and $R_{off} = \sum_{i=1}^{N} R_{d,i}$. In view of the symmetric arrangement of the exciter transformer a further simplification can be achieved by introducing an invertible state transformation in the form $i_\Sigma = i_{p1} + i_{p2}$, $i_\Delta = i_{p1} - i_{p2}$ and $i_r = i_r$. The differential equations of the currents i_Σ, i_r, i_Δ result in

$$\mathbf{L}_{\Sigma r}\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_r \\ i_\Sigma \end{bmatrix} = -\mathbf{R}_{\Sigma r}\begin{bmatrix} i_r \\ i_\Sigma \end{bmatrix} + \begin{bmatrix} u_{dm} + u_l \\ u_\Sigma \end{bmatrix} \tag{1a}$$

$$L_p\frac{\mathrm{d}}{\mathrm{d}t}i_\Delta = -R_p i_\Delta + u_\Delta, \tag{1b}$$

with the new system inputs $u_\Sigma = u_{p1} + u_{p2}$ and $u_\Delta = u_{p1} - u_{p2}$, the demodulator voltage u_{dm}, the output voltage u_l, and the reduced inductance and resistance matrices $\mathbf{L}_{\Sigma r}$ and $\mathbf{R}_{\Sigma r}$. The equations of the voltages u_{dm} and u_l are written as

$$\mathbf{C}\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} u_{dm} \\ u_l \end{bmatrix} = \begin{bmatrix} -i_r - i_{R_{dm}} \\ -i_r - \frac{u_l}{R_l} \end{bmatrix}, \tag{2}$$

with the current $i_{R_{dm}}$ through the resistive part of the demodulator, the capacitance matrix $\mathbf{C}$ and the resistance R_l given by the sum of the resistance of the high-voltage cable and the resistance of the resistor divider at the output of the DRT system, see Figure 1. For the calculation of $i_{R_{dm}}$ and the matrices $\mathbf{L}_{\Sigma r}$, $\mathbf{R}_{\Sigma r}$ and $\mathbf{C}$, the reader is referred to Appendix A and Kemmetmüller et al. (2014).

As described in Section 2.1, the test voltage u_l is basically generated by a defined demodulation of the amplitude modulated resonant voltage u_r. Thus, u_l is mainly affected by the amplitude $\hat{U}_r$, i.e. the low-frequency envelope of the resonant voltage u_r, and not by its high-frequency components. Because of this, it is reasonable to develop an envelope model which describes the time evolution of the envelopes, i.e. the time profile of the mean value and the amplitude of the high frequency signal, see, e.g., Caliskan et al. (1996); Sanders and Verhulst (1985); Egretzberger and Kugi (2010). In order to do so, each of the system states $\mathbf{x}^{\mathrm{T}} = \begin{bmatrix} i_r & i_\Sigma & i_\Delta & u_{dm} & u_l \end{bmatrix}$ and system inputs $\mathbf{u}^{\mathrm{T}} = \begin{bmatrix} u_\Sigma & u_\Delta \end{bmatrix}$ of the mathematical model (1)-(2) are described by a slowly time varying mean component, a cosine component and a sine component in the form

$$r(t) = R_0(t) + R_c(t)\cos(\omega_r t) + R_s(t)\sin(\omega_r t), \tag{3}$$

with $r(t) \in \{\mathbf{x}, \mathbf{u}\}$ and the new envelope components

$$\mathbf{R}(t) = \begin{bmatrix} R_0(t) & R_c(t) & R_s(t) \end{bmatrix} = \begin{bmatrix} R_0(t) & \tilde{\mathbf{R}}(t) \end{bmatrix}. \tag{4}$$

Using this description, the envelope model of the currents i_r, i_Σ and i_Δ results in

$$\mathbf{L}_{\Sigma r}\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} \mathbf{I}_r \\ \mathbf{I}_\Sigma \end{bmatrix} = -\mathbf{L}_{\Sigma r}\begin{bmatrix} \mathbf{I}_r \\ \mathbf{I}_\Sigma \end{bmatrix}\mathbf{\Omega} - \mathbf{R}_{\Sigma r}\begin{bmatrix} \mathbf{I}_r \\ \mathbf{I}_\Sigma \end{bmatrix} + \begin{bmatrix} \mathbf{U}_{dm} + \mathbf{U}_l \\ \mathbf{U}_\Sigma \end{bmatrix} \tag{5a}$$

$$L_p\frac{\mathrm{d}}{\mathrm{d}t}\mathbf{I}_\Delta = -L_p\mathbf{I}_\Delta\mathbf{\Omega} - R_p\mathbf{I}_\Delta + \mathbf{U}_\Delta, \tag{5b}$$

with $\mathbf{\Omega}$ given by

$$\mathbf{\Omega} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & -\omega_r \\ 0 & \omega_r & 0 \end{bmatrix} = \begin{bmatrix} 0 & \mathbf{0} \\ \mathbf{0} & \tilde{\mathbf{\Omega}} \end{bmatrix}. \tag{6}$$

The envelope model of the voltages u_{dm} and u_l can be written according to (2) in the form

$$\begin{aligned}\mathbf{C}\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} \mathbf{U}_{dm} \\ \mathbf{U}_l \end{bmatrix} = &-\mathbf{C}\begin{bmatrix} \mathbf{U}_{dm} \\ \mathbf{U}_l \end{bmatrix}\mathbf{\Omega} - \begin{bmatrix} \mathbf{I}_r + \mathbf{I}_{R_{dm}} \\ \mathbf{I}_r \end{bmatrix} \\ &- \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{R_l} \end{bmatrix}\begin{bmatrix} \mathbf{U}_{dm} \\ \mathbf{U}_l \end{bmatrix}\end{aligned} \tag{7}$$

with the current $\mathbf{I}_{R_{dm}}$ through the resistive part of the demodulator given by

$$\begin{aligned}\mathbf{I}_{R_{dm}} = &\frac{1}{R_{off}}\mathbf{U}_{dm} + \left(\frac{1}{R_{dm}^{+}} - \frac{1}{R_{off}}\right)\mathbf{G}^{+} \\ &+ \left(\frac{1}{R_{dm}^{-}} - \frac{1}{R_{off}}\right)\mathbf{G}^{-}.\end{aligned} \tag{8}$$

with $\mathbf{G}^{-} = \begin{bmatrix} G_0^{-} & G_c^{-} & G_s^{-} \end{bmatrix}$ and $\mathbf{G}^{+} = \begin{bmatrix} G_0^{+} & G_c^{+} & G_s^{+} \end{bmatrix}$. The calculation of the envelope components of $\mathbf{G}^{-}$ and $\mathbf{G}^{+}$ and the envelope description of the input voltages u_Σ and u_Δ is summarized in Appendix A and are discussed in detail in Kemmetmüller et al. (2014).

3. Controller design

Before starting with the controller design, the DRT system with its simplest demodulation strategy is considered. In the simplest demodulation strategy, all thyristors of the positive branch are switched on for the positive half-wave and all thyristors of the negative branch for the negative half-wave of the desired output voltage u_l. As already discussed in Eberharter et al. (2014), this demodulation strategy leads to a significant deviation in u_l from the desired sinusoidal output voltage, especially for large values of C_l. Figure 4 depicts the simulation result of this demodulation strategy for a capacitive load of $C_l = 400\,\mathrm{nF}$. For this simulation, the mathematical model of Section 2.2 was implemented in MATLAB/SIMULINK with the parameters given in Table 2 of Section 5.

As can be seen, the resulting output voltage exhibits a high residual voltage when switching from the positive to the negative half-wave. Beside the deviation from the desired sinusoidal shape, this large residual voltage would also lead to a damage of the high-voltage thyristors in the demodulator. In order to avoid these problems, a suitable control strategy for the test voltage u_l, respectively its

Post-print version of the article: W. Kemmetmüller, S. Eberharter, and A. Kugi, "Controller design and experimental validation of a very low frequency high-voltage test system", *Control Engineering Practice*, vol. 37, pp. 32–42, Apr. 2015. DOI: 10.1016/j.conengprac.2014.12.011
The content of this post-print version is identical to the published paper but without the publisher's final layout or copy editing.

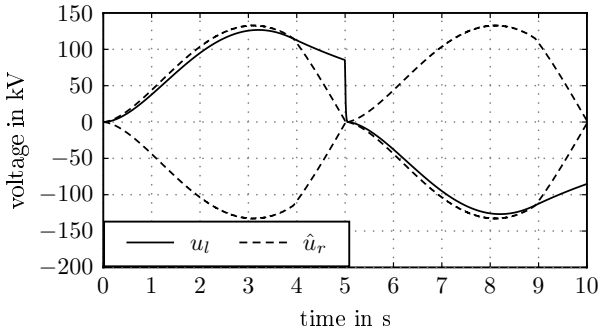

Figure 4: Simplest demodulation strategy with $C_l = 400\,\mathrm{nF}$ and $\chi = 0.15\sin(\omega_\Delta t)$.

mean value $U_{l,0}$, is needed. The test voltage u_l can be controlled by a defined loading and discharging of the cable capacitance C_l by means of the mean current $I_{R_{dm,0}}$ of the demodulator. The current $I_{R_{dm,0}}$ can be adjusted by the pulse width χ of the input voltages, which corresponds to the amplitude $\hat{U}_r$, and the values of the demodulator resistors R^+_{dm} and R^-_{dm}.

The controller design presented in this paper is based on the results of a detailed system analysis and a static optimization problem presented in Kemmetmüller et al. (2014). Therein, the optimization problem was used to calculate an optimal virtual input $(\mathbf{u}^*)^{\mathrm{T}} = \begin{bmatrix}\hat{U}_r^* & R_{dm}^{+,*} & R_{dm}^{-,*}\end{bmatrix}$, which minimizes the THD of the output voltage u_l and the power losses of the DRT system. For the formulation of this optimization problem, two major simplifications were made: First, it was presumed that the resonant voltage u_r ideally tracks a desired voltage u_r^d and that u_r can be directly used as a control input. Second, the overall demodulator was described by a continuously adjustable resistor $R_{dm}(t)$, neglecting the modular design and the physical constraints of the demodulator (see Eberharter et al. (2014)).

In the real DRT system, none of the simplifying assumptions is fulfilled. The resonant voltage u_r cannot be directly used as a control input because it is generated by a suitable choice of the pulse width χ of the power module voltages u_{p1} and u_{p2}. Furthermore, the modular design of the demodulator reduces the possible values of the demodulator resistors R^+_{dm} and R^-_{dm} to a set of only $N+1$ discrete values. In addition to this, the following two problems have to be addressed in the controller design: First, the dielectric strength of the high-voltage thyristors limits the degrees of freedom in the switching off the thyristors and, therefore, must be considered in the calculation of the control inputs. Second, the exact value of the capacitance of the high-voltage cables is generally unknown before the cable testing. For that reason the controller is augmented by an estimator for C_l, which is derived in Section 4.

The controller design now proceeds in the following steps: First, the current $I_{R_{dm,0}}$ is used to formulate a control law, which controls the amplitude and shape of $U_{l,0}$. In order to do so, a two degrees-of-freedom control structure is employed, comprising a feedforward part $I^d_{R_{dm,0}}$ and a feedback part $I^c_{R_{dm,0}}$. Afterwards the real control inputs χ, R^+_{dm} and R^-_{dm} are calculated.

3.1. Control law for virtual control input

If $I_{R_{dm,0}}$ is introduced as a virtual control input of the DRT system and assuming that $U_{r,0}$ is negligibly small, i.e., $U_{dm,0} = -U_{l,0}$, the feedforward control $I^d_{R_{dm,0}}$ of $U_{l,0}$ can be derived from (7) in the form

$$I^d_{R_{dm,0}} = (C_{dm} + \hat{C}_l)\dot{U}^d_{l,0} + \frac{1}{R_l}U^d_{l,0}. \tag{9}$$

Therein, $U^d_{l,0}$ is the desired sinusoidal test voltage and $\hat{C}_l$ is the estimated cable capacitance. The tracking error $e_l = U_{l,0} - U^d_{l,0}$ is stabilized by a PI-controller of the form

$$I^c_{R_{dm,0}} = \left(-\hat{C}_\Sigma k_P + \frac{1}{R_l}\right)e_l - \hat{C}_\Sigma k_I \underbrace{\int_{t_0}^{t} e_l(\tau)\mathrm{d}\tau}_{e_{l,I}}, \tag{10}$$

with the constant controller parameters $k_P, k_I > 0$ and $\hat{C}_\Sigma = C_{dm} + \hat{C}_l$. By use of the control law $I_{R_{dm,0}} = I^d_{R_{dm,0}} + I^c_{R_{dm,0}}$, the overall closed-loop error system can be written in the form

$$\frac{\mathrm{d}}{\mathrm{d}t}e_{l,I} = e_l \tag{11a}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}e_l = \frac{\hat{C}_\Sigma}{C_\Sigma}\left(-k_P e_l - k_I e_{l,I}\right) - \frac{\tilde{C}_l}{C_\Sigma}\dot{U}^d_{l,0}, \tag{11b}$$

with $C_\Sigma = C_{dm} + C_l$ and the estimation error of the cable capacitance $\tilde{C}_l = C_l - \hat{C}_l$. The dynamics of the (linear) error system (11) can be arbitrarily assigned by the two controller parameters k_P and k_I. Obviously, the error e_l converges exponentially to zero if the estimation error for the load capacitance is zero, i.e. $\tilde{C}_l = 0$. If $\tilde{C}_l \neq 0$, an approximation of the resulting error can be obtained by calculating the quasi stationary solution of (11) for a desired sinusoidal output voltage and nominal values of C_l and C_{dm}. For a typical example with $\hat{C}_l = 525\,\mathrm{nF}$, $C_l = 500\,\mathrm{nF}$, $C_{dm} = 0.5\,\mathrm{nF}$, $k_P = 50$, $k_I = 500$ and a sinusoidal output voltage $U^d_{l,0} = \hat{U}^d_{l,0}\sin(2\pi 0.1t)$ with $\hat{U}^d_{l,0} = 200\,\mathrm{kV}$, the error e_l is less than 4‰ of the amplitude of the sinusoidal output voltage.

3.2. Calculation of control inputs χ, R^+_{dm}, R^-_{dm}

This section deals with the calculation of the control inputs χ, R^+_{dm} and R^-_{dm}, which are needed to generate the required demodulator current $I_{R_{dm,0}} = I^d_{R_{dm,0}} + I^c_{R_{dm,0}}$ given by (9) and (10). To understand the influence of χ, R^+_{dm} and R^-_{dm} on $I_{R_{dm,0}}$, the functional principle of the control concept is shortly explained using Figure 5. As can be seen, the control concept is divided into two control phases, i.e. a loading phase $\mathbf{A}^+$ and a discharging phase $\mathbf{B}^+$ of the cable capacitance, with the superscript $'+'$ referring to the positive half-wave. The choice of these two

Post-print version of the article: W. Kemmetmüller, S. Eberharter, and A. Kugi, "Controller design and experimental validation of a very low frequency high-voltage test system", *Control Engineering Practice*, vol. 37, pp. 32–42, Apr. 2015. DOI: 10.1016/j.conengprac.2014.12.011
The content of this post-print version is identical to the published paper but without the publisher's final layout or copy editing.

control phases was mainly influenced by the result of the optimization problem presented in Kemmetmüller et al. (2014). Because of the symmetry of the demodulator and for reasons of brevity, the description of the control phases and the calculation of the control inputs for each phase will be illustrated for the positive half-wave of u_l only:

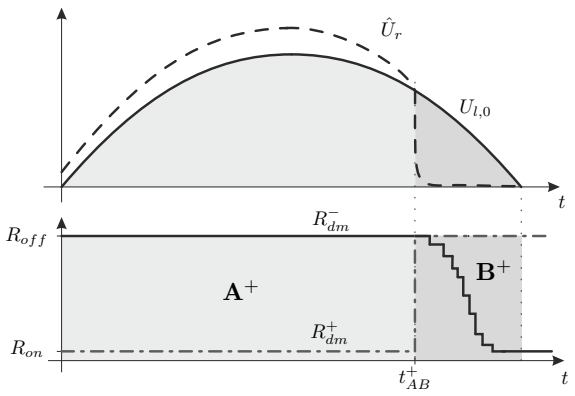

Figure 5: Control phases $\mathbf{A}^+$ and $\mathbf{B}^+$ for the positive half-wave of $U_{l,0}$.

- **Phase $\mathbf{A}^+$**: C_l is loaded by the demodulator current $I_{R_{dm,0}}$ and $U_{l,0}$ is only controlled via the power module by suitably adjusting the pulse width χ. The demodulator resistors take the constant values $R_{dm}^+ = R_{on}$ and $R_{dm}^- = R_{off}$. This control phase is characterized by the condition $\hat{U}_r \geq U_{l,0}$.
- **Phase $\mathbf{B}^+$**: C_l is discharged to prevent a high residual voltage at the transition from the positive to the negative half-wave. $U_{l,0}$ is only controlled by the demodulator resistor R_{dm}^-, while R_{dm}^+ is set to $R_{dm}^+ = R_{off}$ and the resonant voltage to zero, i.e., $\chi = 0$. Due to the vanishing resonant voltage, the power losses in the DRT system are minimized. In this control phase, the value of R_{dm}^- is determined by a defined switching of the thyristors in the demodulator considering its modular design and the dielectric strength of the high-voltage thyristors.

3.2.1. Calculation of χ in phase $\mathbf{A}^+$

The calculation of χ in phase $\mathbf{A}^+$ consists of several steps. First, the amplitude $\hat{U}_{dm}$ of the demodulator voltage is calculated based on the demodulator current $I_{R_{dm,0}}$. In order to do so, (8) is solved for G_0^+, with the assumption $U_{r,0} = 0$ introduced in Section 3.1 and the demodulator resistors $R_{dm}^+ = R_{on}$ and $R_{dm}^- = R_{off}$,

$$G_0^+(\hat{U}_{dm}, U_{dm,0}) \approx G_0^+(\hat{U}_{dm}, -U_{l,0}^d) = \frac{I_{R_{dm,0}} + \frac{U_{l,0}^d}{R_{off}}}{\frac{1}{R_{on}} - \frac{1}{R_{off}}}. \tag{12}$$

This equation can be numerically solved for $\hat{U}_{dm}$, using G_0^+ from (36), a desired sinusoidal output voltage $U_{l,0}^d = \hat{U}_{l,0}\sin(\omega_\Delta t)$, and the demodulator current $I_{R_{dm,0}}$ according to (9)-(10).

In a next step, $\hat{U}_{dm}$ is used to calculate the amplitude $\hat{U}_\Sigma = \sqrt{U_{\Sigma,c}^2 + U_{\Sigma,s}^2}$ of the input voltage $\mathbf{U}_\Sigma$, which is a function of the control input χ (33). An investigation of (5a) and (7) shows that the dynamics of the sine and cosine envelope components are much faster than the dynamics of the mean values. Thus, for the further calculation, a quasi-stationary formulation of (5a) and (7) with (38), i.e.

$$\mathbf{0} = -\mathbf{L}_{\Sigma r}\begin{bmatrix}\tilde{\mathbf{I}}_r\\ \tilde{\mathbf{I}}_\Sigma\end{bmatrix}\tilde{\Omega} - \mathbf{R}_{\Sigma r}\begin{bmatrix}\tilde{\mathbf{I}}_r\\ \tilde{\mathbf{I}}_\Sigma\end{bmatrix} + \begin{bmatrix}\tilde{\mathbf{U}}_{dm} + \tilde{\mathbf{U}}_l\\ \tilde{\mathbf{U}}_\Sigma\end{bmatrix} \tag{13a}$$

$$\mathbf{0} = -\mathbf{C}\begin{bmatrix}\tilde{\mathbf{U}}_{dm}\\ \tilde{\mathbf{U}}_l\end{bmatrix}\tilde{\Omega} - \begin{bmatrix}\tilde{\mathbf{I}}_r - \Psi\tilde{\mathbf{U}}_{dm}\\ \tilde{\mathbf{I}}_r\end{bmatrix} - \begin{bmatrix}0 & 0\\ 0 & \frac{1}{R_l}\end{bmatrix}\begin{bmatrix}\tilde{\mathbf{U}}_{dm}\\ \tilde{\mathbf{U}}_l\end{bmatrix} \tag{13b}$$

can be considered.

For the solution of (13), a transformation of all cosine and sine components to their amplitude and phase angle is introduced

$$\begin{aligned}
U_{\Sigma,c} &= \hat{U}_\Sigma\cos(\phi), & U_{\Sigma,s} &= \hat{U}_\Sigma\sin(\phi)\\
U_{dm,c} &= \hat{U}_{dm}\cos(\phi+\phi_{dm}), & U_{dm,s} &= \hat{U}_{dm}\sin(\phi+\phi_{dm})\\
U_{l,c} &= \hat{U}_l\cos(\phi+\phi_l), & U_{l,s} &= \hat{U}_l\sin(\phi+\phi_l)\\
I_{r,c} &= \hat{I}_r\cos(\phi+\phi_r), & I_{r,s} &= \hat{I}_r\sin(\phi+\phi_r)\\
I_{\Sigma,c} &= \hat{I}_\Sigma\cos(\phi+\phi_\Sigma), & I_{\Sigma,s} &= \hat{I}_\Sigma\sin(\phi+\phi_\Sigma).
\end{aligned} \tag{14}$$

If additionally the differential angles $\Delta\phi_{dm,l} = \phi_{dm} - \phi_l, \Delta\phi_{r,l} = \phi_r - \phi_l, \Delta\phi_{\Sigma,l} = \phi_\Sigma - \phi_l$ are introduced and the value of $\hat{U}_{dm}$ from (12) is inserted into (13) and (14), the system of equations (13) can be solved for the unknowns $\hat{U}_l, \Delta\phi_{dm,l}, \hat{I}_r, \Delta\phi_{r,l}, \hat{I}_\Sigma, \Delta\phi_{\Sigma,l}, \hat{U}_\Sigma$ and ϕ_l. Finally, the amplitude $\hat{U}_\Sigma$ of the new system input results in

$$\begin{aligned}
\hat{U}_\Sigma =& R_p\hat{I}_\Sigma\cos(\phi_l + \Delta\phi_{\Sigma,l}) + \omega_r L_p\hat{I}_\Sigma\sin(\phi_l + \Delta\phi_{\Sigma,l})\\
&+ 2\omega_r L_{ps}\hat{I}_r\sin(\phi_l + \Delta\phi_{r,l}).
\end{aligned} \tag{15}$$

A detailed calculation of all unknowns in (13) can be found in the Appendix. Combining (15) with (33), the required control input χ in phase $\mathbf{A}^+$ can be analytically calculated in the form

$$\chi = \arctan\left(\frac{\sqrt{-\pi^4\hat{U}_\Sigma^2 + (8u_p\pi)^2}}{u_p^2}, \frac{32u_p^2 - \hat{U}_\Sigma^2\pi^2}{u_p^2}\right). \tag{16}$$

3.2.2. Calculation of R_{dm}^- in phase $\mathbf{B}^+$

In phase $\mathbf{B}^+$, the pulse width χ is set to zero and the thyristors in the positive branch are switched off, i.e., $R_{dm}^+ = R_{off}$. Consequently, only the value of R_{dm}^- is used as a control input in this phase.

Post-print version of the article: W. Kemmetmüller, S. Eberharter, and A. Kugi, "Controller design and experimental validation of a very low frequency high-voltage test system", *Control Engineering Practice*, vol. 37, pp. 32–42, Apr. 2015. DOI: 10.1016/j.conengprac.2014.12.011
The content of this post-print version is identical to the published paper but without the publisher's final layout or copy editing.

For a continuously adjustable demodulator resistor the required value of $R_{dm}^{-}(t)$ could be directly calculated by

$$R_{dm}^{-}(t) = -\frac{U_{l,0}^{d}}{I_{R_{dm,0}}}, \tag{17}$$

with the desired sinusoidal output voltage $U_{l,0}^{d}$ and $I_{R_{dm,0}} = I_{R_{dm,0}}^{d} + I_{R_{dm,0}}^{c}$ given by the control law (9)-(10). Because of the modular design of the demodulator, the desired resistance $R_{dm}^{-}(t)$ can only be approximated by a defined switching of the high-voltage thyristors. The current hardware only allows a sequential switching of the demodulator modules, where each module can be switched on once during the discharging phase $\mathbf{B}^{+}$. This restriction leads to a set of $N+1$ possible resistance values in the form

$$R_{dm,i}^{-} = \begin{cases} \sum_{l=1}^{N} R_{d,l} & \text{if } i = 0 \\ \sum_{k=1}^{i} \tilde{R}_{lo,k} + \sum_{l=i+1}^{N} R_{d,l} & \text{if } i = 1,\ldots,N-1 \\ \sum_{k=1}^{N} \tilde{R}_{lo,k} & \text{if } i = N, \end{cases} \tag{18}$$

with $R_{lo,1} = R_{lo,2} = \ldots = R_{lo,N}$ and $R_{d,1} \geq R_{d,2} \geq R_{d,N}$, see Table 2 of Section 5. The subscript i in (18) refers to the number of demodulator modules which are switched on and $\tilde{R}_{lo,k} = R_{lo,k}||R_{d,k}$. As the value of the discharge resistor $R_{d,k}$ is more than 200 times larger than the value of $R_{lo,k}$, the following assumption $\tilde{R}_{lo,k} \approx R_{lo,k}$ can be made. In addition to the modular design of the demodulator, the dielectric strength of the high-voltage thyristors has to be taken into account. Switching to a configuration i is only permitted when the condition

$$\frac{R_{d,i+1}}{R_{dm,i}^{-}} U_{l,0} \leq U_{dm,max}, \tag{19}$$

with the maximum voltage $U_{dm,max}$ allowed for each demodulator module, is fulfilled. Based on these considerations, the calculation of the number i of modules to be switched on proceeds along the following steps: (i) The theoretically necessary value of $R_{dm}^{-}(t)$ is calculated by (17). (ii) If the error $e_l = U_{l,0} - U_{l,0}^{d}$ is positive, i.e. $e_l > 0$, the number i of modules to be switched on is calculated such that the corresponding resistance $R_{dm,i}^{-}$ is the closest possible value smaller than $R_{dm}^{-}(t)$. If the condition (19) is not fulfilled for the calculated i, the demodulator cannot be switched and the demodulator resistance R_{dm}^{-} is kept at its actual value.

3.2.3. Calculation of the switching time t_{AB}^{+}

In order to complete the controller design, the conditions for a correct switching between the control phases have to be determined. A detailed analysis of the nonlinear terms G_0^{+} and G_0^{-} shows that in phase $\mathbf{A}^{+}$, G_0^{+} is always positive and G_0^{-} takes values smaller than zero, whereas in phase $\mathbf{B}^{+}$, $G_0^{+} < 0$ and $G_0^{-} < 0$. Thus, it is obvious that the switching between the control phases can be detected by the change of sign in the nonlinear terms $G_0^{\pm}$. The resulting switching conditions are summarized in Table 1 with the nonlinear terms $G_0^{\pm}$ calculated from (12) and (37) with the demodulator current $I_{R_{dm,0}}$ given by (9),(10). In order to achieve a more robust switching from the discharging phases to the loading phases, i.e., $\mathbf{B}^{+} \rightarrow \mathbf{A}^{-}$ and $\mathbf{B}^{-} \rightarrow \mathbf{A}^{+}$, the switching is performed at the zeros of the desired output voltage $U_{l,0}^{d}$.

phase	G_0^{+}	G_0^{-}
$\mathbf{A}^{+}$	≥ 0	< 0
$\mathbf{B}^{+}$	< 0	< 0
$\mathbf{A}^{-}$	< 0	≥ 0
$\mathbf{B}^{-}$	> 0	> 0

Table 1: Switching condition for the control phases.

Remark 1. *For a sinusoidal output voltage $U_{l,0} = \hat{U}_{l,0}\sin(\omega_\Delta t)$ and known cable parameters R_l and C_l, the switching time t_{AB}^{+} from $\mathbf{A}^{+} \rightarrow \mathbf{B}^{+}$ could be calculated from the condition $G_0^{+} = 0$ in the form*

$$t_{AB}^{+} = \frac{1}{\omega_\Delta}\left(\arctan\left(-\frac{\omega_\Delta C_l}{\frac{1}{R_{off}} + \frac{1}{R_l}}\right) + \pi\right), \tag{20}$$

see Kemmetmüller et al. (2014). Due to uncertainties in the parameters R_l and C_l, this approach however, is not suitable for a practical implementation of the proposed control concept.

4. Estimation of the cable capacitance C_l

This section deals with the development of an estimator for the unknown cable capacitance C_l, which is required for the implementation of the control strategy (9)-(10).

For the development of the estimator two simplifications are made: (i) It is assumed that the resistance R_l of the load (given by the cable resistance in parallel to the resistance of the voltage divider) is known. This assumption is meaningful since the resistance of the cable is typically much higher than the resistance of the voltage divider. Thus, R_l can be set to this value, which of cause is well known. (ii) It is expected that the value of the cable capacitance C_l does not vary significantly during the cable test operation.

Because of the second simplification, it is sufficient to estimate C_l only once before the start of the cable test. In order to do so, the high-voltage cable is loaded to a defined voltage level and subsequently discharged by a constant discharge resistance, see Figure 6. As can be seen, the resonant voltage u_r is set to zero during the discharging of C_l, i.e., $\chi = 0$. This, leads to a reduction of the disturbances in the measurement of u_l, which are mainly caused by the switching of the full-bridges in the power module. Additionally, $u_r = 0$ yields $u_{dm} = -u_l$ and thus u_l in (2)

Post-print version of the article: W. Kemmetmüller, S. Eberharter, and A. Kugi, "Controller design and experimental validation of a very low frequency high-voltage test system", *Control Engineering Practice*, vol. 37, pp. 32–42, Apr. 2015. DOI: 10.1016/j.conengprac.2014.12.011
The content of this post-print version is identical to the published paper but without the publisher's final layout or copy editing.

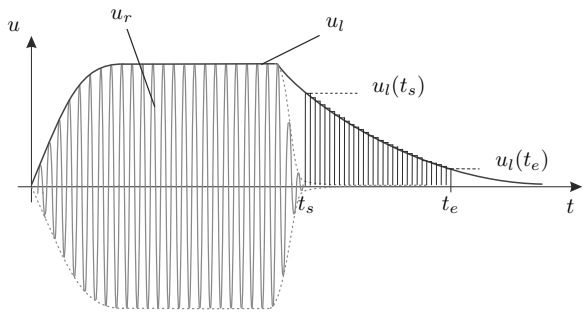

Figure 6: Functional principle of estimation of C_l.

can be simplified to

$$\frac{\mathrm{d}}{\mathrm{d}t}u_l = -\frac{1}{C_\Sigma}\left(\frac{1}{R^-_{dm,n}} + \frac{1}{R_l}\right)u_l, \tag{21}$$

with $C_\Sigma = C_{dm} + C_l$ and the constant discharging resistance $R^-_{dm,n}$ for fixed n with $1 \leq n \leq N$, see (18). For the choice of n two facts must be taken into account: (i) A small value of n (corresponding to a large value of $R^-_{dm,n}$) yields a slow discharge. Thus, a large number of measurements can be taken, which is beneficial for the subsequent estimation of C_l. (ii) A large value of n (a small value of $R^-_{dm,n}$) on the other hand reduces the influence of the resistance R_l on the estimation accuracy. Based on these considerations, a choice of approximately $\frac{N}{2}$ proves to be a good compromise.

For the development of the proposed estimator for C_l, (21) is integrated over the time t, which results in

$$u_l(t) = u_l(t_s) - \underbrace{\frac{1}{C_\Sigma}\left(\frac{1}{R^-_{dm,n}} + \frac{1}{R_l}\right)\int_{t_s}^{t} u_l \mathrm{d}t}_{\Delta Q}. \tag{22}$$

For the implementation of the estimation algorithm on a real-time hardware, the integral in (22) is approximated by

$$\Delta Q_k = \begin{cases} 0, & \text{if} \quad k = n_s \\ T_m\left(\frac{1}{R^-_{dm,n}} + \frac{1}{R_l}\right)\sum_{j=n_s}^{k-1} u_{l,j} & \text{if} \quad k = n_s+1,\ldots,n_e, \end{cases} \tag{23}$$

with the measurement index k, the measurement sampling time for the estimation T_m, and the indices n_s and n_e corresponding to the measurement times t_s and t_e, respectively. Using ΔQ_k from (23), the k-th measurement of u_l can be written according to (22) in the form

$$u_{l,k} = u_{l,n_s} - \frac{1}{C_\Sigma}\Delta Q_k, \quad k = n_s,\ldots,n_e. \tag{24}$$

In order to obtain an estimation of C_l that is robust against measurement noise, a least-squares approach is employed. For this purpose, (24) is rewritten in vector notation resulting in

$$\underbrace{\begin{bmatrix} u_{l,n_s} \\ u_{l,n_s+1} \\ \vdots \\ u_{l,n_e} \end{bmatrix}}_{\mathbf{y}} = \underbrace{\begin{bmatrix} 1 & -\Delta Q_{n_s} \\ 1 & -\Delta Q_{n_s+1} \\ \vdots & \\ 1 & -\Delta Q_{n_e} \end{bmatrix}}_{\mathbf{S}} \underbrace{\begin{bmatrix} u_{l,n_s} \\ (C_\Sigma)^{-1} \end{bmatrix}}_{\mathbf{p}}, \tag{25}$$

with the measurement vector $\mathbf{y} \in \mathbb{R}^{n_e-n_s+1}$, the regression matrix $\mathbf{S} \in \mathbb{R}^{(n_e-n_s+1)\times 2}$ and the parameter vector $\mathbf{p} \in \mathbb{R}^2$. The best approximation of $\mathbf{p}$ in the least-squares sense is then given by

$$\hat{\mathbf{p}} = \begin{bmatrix} \hat{u}_{l,n_s} \\ (\hat{C}_\Sigma)^{-1} \end{bmatrix} = \left(\mathbf{S}^T\mathbf{S}\right)^{-1}\mathbf{S}^T\mathbf{y}. \tag{26}$$

Thus, $\hat{C}_l$ can be calculated from (26) and the value of the demodulator capacitance C_{dm}.

The estimation quality of C_l depends on the accuracy of C_{dm}, $R^-_{dm,n}$ and R_l. In normal operation, the resistance R_l, which is defined by the value of the resistive voltage divider and the resistance of the high-voltage cable, is not exactly known since it can vary with the condition of the cable isolation, see, e.g, J. Hernandez-mejia, R. Harley, N. Hampton, R. Hartlein (2009); J. Perkel, Y. Del Valle, R.N. Hampton, J.C. Hernandez-mejia, J. Densley (2013). Furthermore, the simplification of the capacitance network in the demodulator in form of the parallel capacitance C_{dm} can cause further estimation errors. However, as will be shown in the simulation results, the estimation concept in combination with the proposed control strategy is robust with respect to these errors.

5. Simulation results

In this section, several simulations are presented: First, the behavior of the DRT system is analyzed for the case where the cable capacitance cannot be completely discharged during the discharging phases $\mathbf{B}^{\pm}$. Second, the influence of variations in R_l and the simplification of the demodulator model on the estimation accuracy of C_l will be discussed for two different cable capacitances.

For the simulations, the control and estimation algorithm presented in the previous sections were implemented in MATLAB/SIMULINK. They are tested on the detailed calibrated mathematical model presented in Eberharter et al. (2014), which comprises a more detailed description of the demodulator and its capacitance network. The controller and model parameters used in the simulations are summarized in Table 2. In the first simulation scenario, the control and estimation strategy is tested for a capacitive load of 760 nF and a desired sinusoidal output voltage with an amplitude $\hat{U}^d_{l,0} = 180\,\mathrm{kVrms}$ and an angular frequency $\omega_\Delta = 2\pi 0.1\,\mathrm{rad\,s^{-1}}$. The result of this simulation is depicted in Figure 7. As can be seen, the output voltage u_l has a residual voltage of approximately 8 kV when

Post-print version of the article: W. Kemmetmüller, S. Eberharter, and A. Kugi, "Controller design and experimental validation of a very low frequency high-voltage test system", *Control Engineering Practice*, vol. 37, pp. 32–42, Apr. 2015. DOI: 10.1016/j.conengprac.2014.12.011
The content of this post-print version is identical to the published paper but without the publisher's final layout or copy editing.

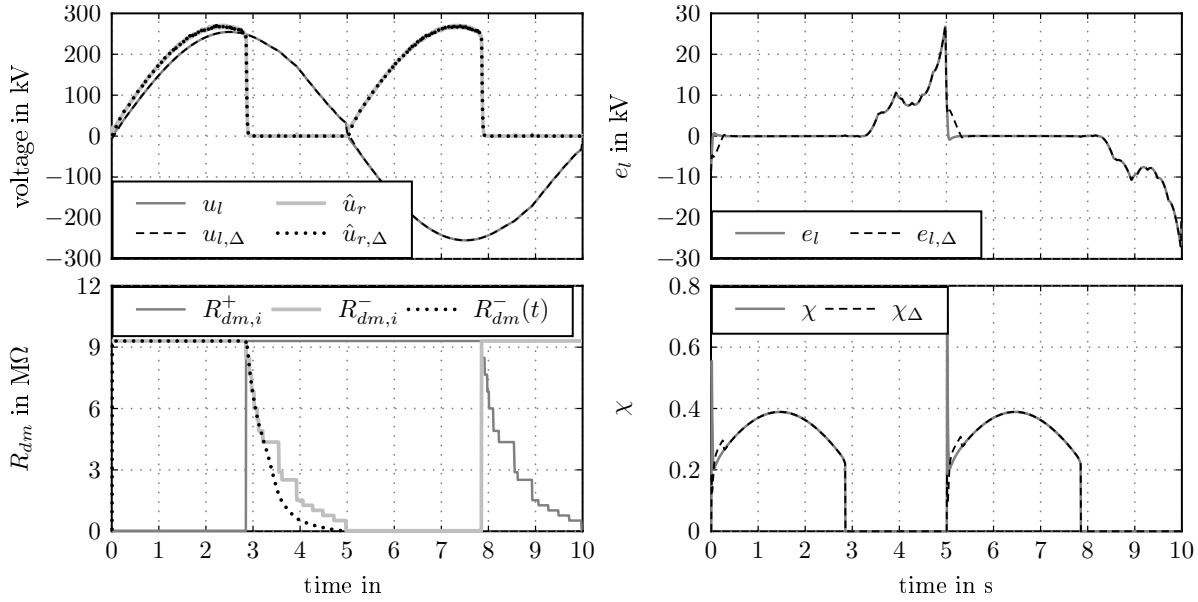

Figure 7: Simulation result for a sinusoidal output voltage with an amplitude of $\hat{U}^d_{l,0} = 180\,\mathrm{kV}$ rms, an angular output frequency of $\omega_\Delta = 2\pi 0.1\,\mathrm{rad\,s^{-1}}$, a capacitive load of $C_l = 760\,\mathrm{nF}$ and $K_\Delta = 25000$.

switching from the positive to the negative half-wave. This residual voltage arises since the discharging resistance R^-_{dm} cannot be reduced fast enough because of the restriction due to the dielectric strength of the thyristors, see $R^-_{dm,i}$ and $R_{dm}(t)^-$ on the bottom left in Figure 7. Now, when switching from the control via the demodulator resistance in phase $\mathbf{B}^\pm$ to the control with the power module by the pulse-width χ, the large error e_l of 8 kV yields large values of χ and thus excessively large currents in the power module. To protect the power module, an automatic shut down will occur. In order to avoid such a shut down, one possible solution would be to slow down the controller by reducing the controller gains k_I and k_P. However, this solution would also worsen the disturbance suppression by the controller and, therefore, another solution is chosen for the proposed controller. The error $e_l = U^d_{l,0} - U_{l,0}$ seen by the controller is manipulated at the switching time in the form

$$\tilde{e}_l = e_l - \Delta e_l. \tag{27}$$

The idea is now to smoothen the switching of the control inputs by setting $\Delta e_l = e_l$ at the switching instant. Afterwards, this value is slowly driven to zero by

$$\Delta e_{l,k+1} = \begin{cases} \Delta e_{l,k} - K_\Delta T_s \operatorname{sign}(e_{l,k}), & \text{if} \quad |\Delta e_{l,k}| > K_\Delta T_s \\ 0 & \text{else,} \end{cases} \tag{28}$$

with the sampling time T_s of the controller and the parameter K_Δ, which has to be chosen depending on the value of the residual voltage and the desired output angular frequency ω_Δ. The simulation results of the control strategy with the modified output error given in (27) is also depicted in Figure 7, where the subscript 'Δ' refers to the modification. Compared to the result of the original control strategy, this measure significantly reduces the peak in the control input χ and, therefore, will be used in the subsequent implementation of the control strategy on the prototype hardware.

The second part of this section is concerned with the analysis of the estimator for the unknown cable capacitance C_l. The estimator is tested by means of two cable capacities $C_l = 1000\,\mathrm{nF}$ and $C_l = 250\,\mathrm{nF}$. In both cases, the value of the cable resistance is changed from $R_l = 300\,\mathrm{M\Omega}$ to $R_l = 100\,\mathrm{M\Omega}$, simulating a defect in the isolation of the test cable, i.e. an increase of the $\tan(\delta)$ value of the cable. For the estimation of C_l, it was assumed that the value of the cable resistance is set to the nominal value of $R_l = 300\,\mathrm{M\Omega}$. The estimation results are given in Table 3. As can be seen, this large variation in R_l results in a negligibly small deviation in $\hat{C}_l$. The estimation error $\tilde{C}_l$ is mainly caused by the simplification of the capacitance network in the demodulator and increases with decreasing values of the cable capacitance C_l. However, in both cases the maximum deviation from the nominal value is less than 1.5 %, which is completely sufficient for the proposed control strategy.

6. Measurement results

In this section measurement results are given in order to prove the practical feasibility of the proposed control and estimation strategy. The control and estimation algorithm was implemented on a DSpace real-time hardware MicroAutobox II and analyzed by measurements on a test

Post-print version of the article: W. Kemmetmüller, S. Eberharter, and A. Kugi, "Controller design and experimental validation of a very low frequency high-voltage test system", *Control Engineering Practice*, vol. 37, pp. 32–42, Apr. 2015. DOI: 10.1016/j.conengprac.2014.12.011
The content of this post-print version is identical to the published paper but without the publisher's final layout or copy editing.

description	symbol	value
primary inductance	L_p	20 mH
secondary inductance	L_s	3.38 H
primary resistance	R_p	3 mΩ
secondary resistance	R_s	0.3 Ω
coupling factor	k	0.9997
resonant frequency	ω_r	$2\,\pi 1\,106\,\mathrm{rad\,s^{-1}}$
resonator capacitance	C_r	5 nF
resonator inductance	L_r	3.5 H
resonator resistance	R_r	520 Ω
demodulator capacitance	C_{dm}	0.91 nF
total discharge resistance	R_{off}	9.3 MΩ
total loading resistance	R_{on}	25 kΩ
SVU discharge resistance	$R_{d,1} \ldots R_{d,4}$	850 kΩ
SVU discharge resistance	$R_{d,5} \ldots R_{d,9}$	550 kΩ
SVU discharge resistance	$R_{d,10} \ldots R_{d,13}$	375 kΩ
SVU discharge resistance	$R_{d,14} \ldots R_{d,20}$	250 kΩ
SVU loading resistance	$R_{lo,1} \ldots R_{lo,20}$	1.25 kΩ
amplitude input voltages	u_p	540 V
sampling time controller	T_s	3 ms
sampling time estimation	T_m	6 ms
start sample	n_s	10
par. controller ($\mathbf{A}^{\pm}$)	k_I	500
par. controller ($\mathbf{A}^{\pm}$)	k_P	50
par. controller ($\mathbf{B}^{\pm}$)	k_I	50
par. controller ($\mathbf{B}^{\pm}$)	k_P	5

Table 2: Model and controller parameters.

$C_l = 1000\,\mathrm{nF}$		
$\hat{C}_l$	R_l	$\tilde{C}_l$
999.6 nF	300 MΩ	0.39 nF
999.3 nF	100 MΩ	−0.68 nF
$C_l = 250\,\mathrm{nF}$		
$\hat{C}_l$	R_l	$\tilde{C}_l$
252.6 nF	300 MΩ	−2.55 nF
252.5 nF	100 MΩ	−2.47 nF

Table 3: Influence of R_l on the estimation accuracy of the cable capacitance C_l.

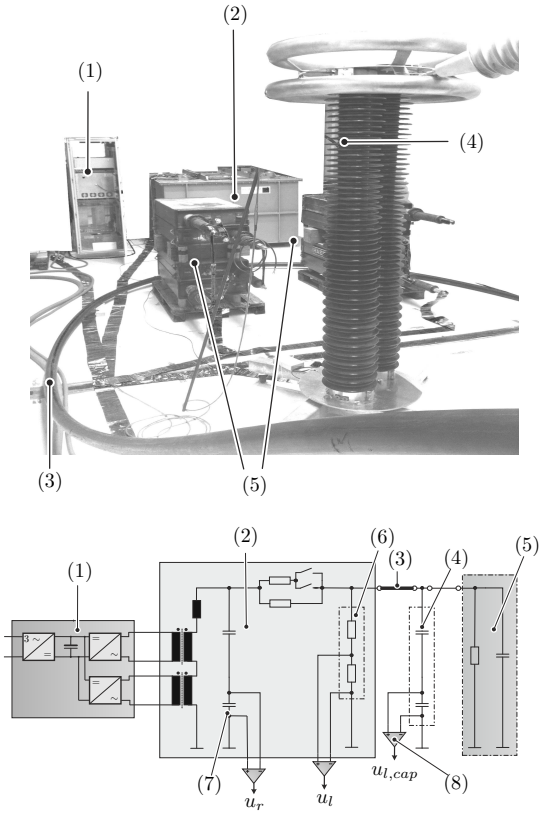

Figure 8: Test bench at the Mohaupt High Voltage facility and the circuit diagram of the DRT system with the measurement set-up: (1) power module, (2) high-voltage container (resonant circuit + SVU), (3) high-voltage connection cable, (4) coupling capacitance with external capacitive divider, (5) high-voltage capacitors (load), (6) internal resistive divider, (7) internal capacitive divider, (8) differential amplifiers.

bench. The test bench was built by the company Mohaupt High Voltage GmbH. It includes a DRT prototype designed for cable tests up to 200 kV rms and an angular frequency range of $2\pi 0.01\,\mathrm{rad\,s^{-1}} \leq \omega_\Delta \leq 2\,\pi 10\,\mathrm{rad\,s^{-1}}$, and high-voltage capacitors, which are used for emulating the high-voltage test cable, see the upper part of Figure 8. The high-voltage capacitors are connected to the DRT system by using a high-voltage connection cable and a coupling capacitor. The coupling capacitor is further used to set up a capacitive voltage divider, which gives an additional measurement for the evaluation of the quality of the test voltage u_l. Since this external voltage divider is not available during a normal cable test operation, the required voltage measurement for the controller is accomplished by an internal resistive divider, see the lower part of Figure 8. The resonant voltage u_r is measured by a capacitive divider given by the resonant capacitance and an additional measurement capacitance. In order to suppress disturbances caused e.g. by the switching of the power module, differential amplifiers were utilized for all measurements. The measured signals were recorded by the DSpace real-time hardware at a sampling rate of $20\,\mathrm{kS\,s^{-1}}$.

The communication between the DSpace real-time hardware and the DRT prototype is accomplished by two serial interfaces. The data between the DSpace system and the power module is transmitted via CAN bus 2.0A at a transfer rate of $250\,\mathrm{kBds^{-1}}$. The switching of the thyristors in the demodulator is controlled via SPI at a transfer rate of $115\,\mathrm{kBds^{-1}}$.

In the first measurement, the proposed control and estimation strategy was tested for a desired sinusoidal output voltage with an amplitude of 35 kV rms, a desired angular test frequency of $\omega_\Delta = 2\pi 0.1\,\mathrm{rad\,s^{-1}}$ and a nominal load capacitance of 500 nF. The estimation of the capacitance results in a value of $\hat{C}_l = 504.8\,\mathrm{nF}$. Figure 9 depicts the measurement results of the voltages u_l and u_r, whereas the output voltage was measured by both, the internal resistive divider denoted by u_l and the external capacitive

Post-print version of the article: W. Kemmetmüller, S. Eberharter, and A. Kugi, "Controller design and experimental validation of a very low frequency high-voltage test system", *Control Engineering Practice*, vol. 37, pp. 32–42, Apr. 2015. DOI: 10.1016/j.conengprac.2014.12.011
The content of this post-print version is identical to the published paper but without the publisher's final layout or copy editing.

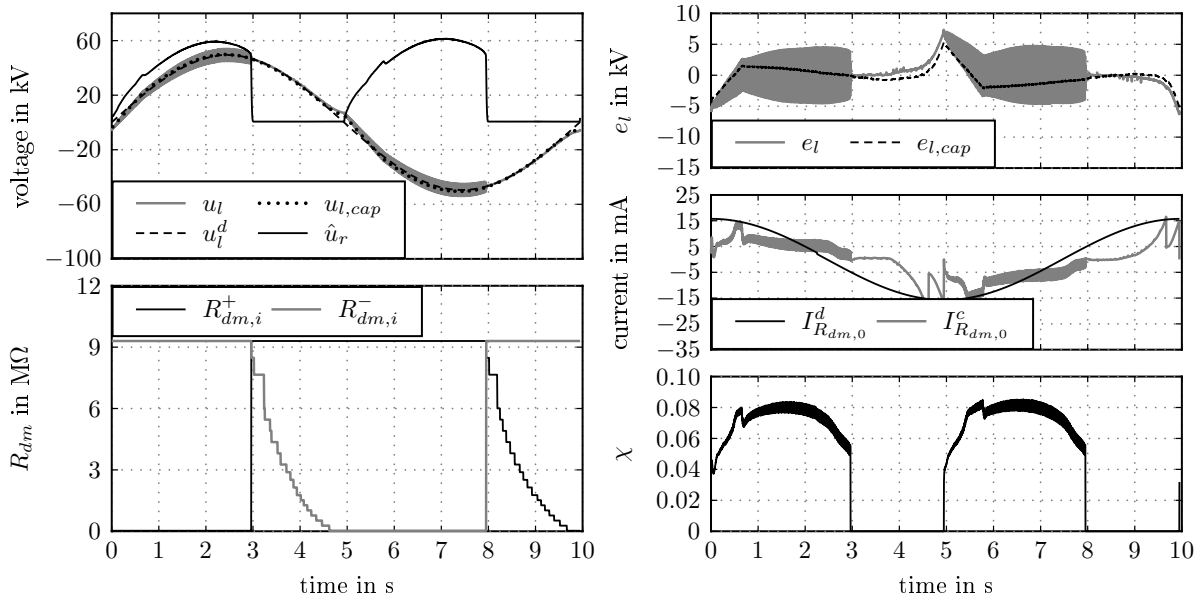

Figure 9: Measurement result for a sinusoidal output voltage with an amplitude of $\hat{U}_{l,0}^d = 35\,\text{kV}$ rms, an angular output frequency of $\omega_\Delta = 2\pi 0.1\,\text{rad}\,\text{s}^{-1}$, an estimated capacitance $\hat{C}_l = 504.8\,\text{nF}$ and $K_\Delta = 8000$.

divider denoted by $u_{l,cap}$. As can be seen from the plots of the voltages u_l and $u_{l,cap}$ and the corresponding output errors e_l and $e_{l,cap}$, an excellent sinusoidal shape is achieved for almost the entire period of u_l^d. Because of the low-pass characteristic of the high-voltage connection cable, the capacitive divider provides a smoother measurement of the output voltage u_l than the internal resistive divider. The feedforward part $I_{R_{dm,0}}^d$ of the virtual control input $I_{R_{dm,0}}$ shows, as expected, a cosine shape, whereas the small feedback current $I_{R_{dm,0}}^c$ is needed to compensate for the inaccuracies in the mathematical model. The small residual voltage at the zero crossings occurred because it was not possible to switch off the last demodulator modules. This results from the fact that the energy for the switching of the thyristors is drawn from the high-frequency resonant voltage, which provides too less energy at low voltage levels. This problem is only present at lower voltage levels and vanishes with increasing resonant voltages, respectively output voltages u_l. Nevertheless, the total harmonic distortion (THD) value of the resulting output voltage is less than 0.5 %, which is more than sufficient compared to the required THD value of less than 5 % for sinusoidal VLF test voltages.

The second measurement, given in Figure 10, shows the robustness of the proposed control and estimation strategy with respect to changes in the load capacitance, the desired angular output test frequency ω_Δ and the desired amplitude $\hat{U}_{l,0}^d$ of the sinusoidal output voltage. As can be seen, the proposed control strategy achieves a very good sinusoidal shape for all test scenarios with THD values of the generated test voltages of less than 0.1 %.

7. Conclusions

In the present work, a model based control concept for a very low frequency (VLF) high-voltage test system based on the so called differential resonance technology (DRT) was developed. First, the functional principle of the VLF test system and a simplified mathematical model was described. Based on this, an envelope model was derived, which served as the basis for the design of the proposed control strategy. It was shown that a suitable control of the DRT system is absolutely necessary in order to meet the high quality standards of the VLF sinusoidal test voltages. A two degrees-of-freedom control structure comprising a feedforward and a feedback controller together with an estimator for the unknown cable capacitance was developed. One of the main advantages of this approach is the systematic model based design of the controller, which allows an easy adaptation of the concept to DRT systems with other voltage levels. The feasibility of the proposed control strategy was shown by several measurement results on a test bench with a DRT prototype for cable tests up to 200 kV rms. The measurement results prove that a high quality VLF test voltage is obtained, with THD values less than 0.1 %. Furthermore, it could be shown that the control strategy makes it possible to easily change the amplitude and frequency of the desired sinusoidal test voltage. Finally, the controller turns out to be robust with respect to changes in the cable capacitance. This has been proven in the measurements by changing the load capacitance in a large range from $C_l = 14\,\text{nF}$ up to $C_l = 500\,\text{nF}$.

Post-print version of the article: W. Kemmetmüller, S. Eberharter, and A. Kugi, "Controller design and experimental validation of a very low frequency high-voltage test system", *Control Engineering Practice*, vol. 37, pp. 32–42, Apr. 2015. DOI: 10.1016/j.conengprac.2014.12.011
The content of this post-print version is identical to the published paper but without the publisher's final layout or copy editing.

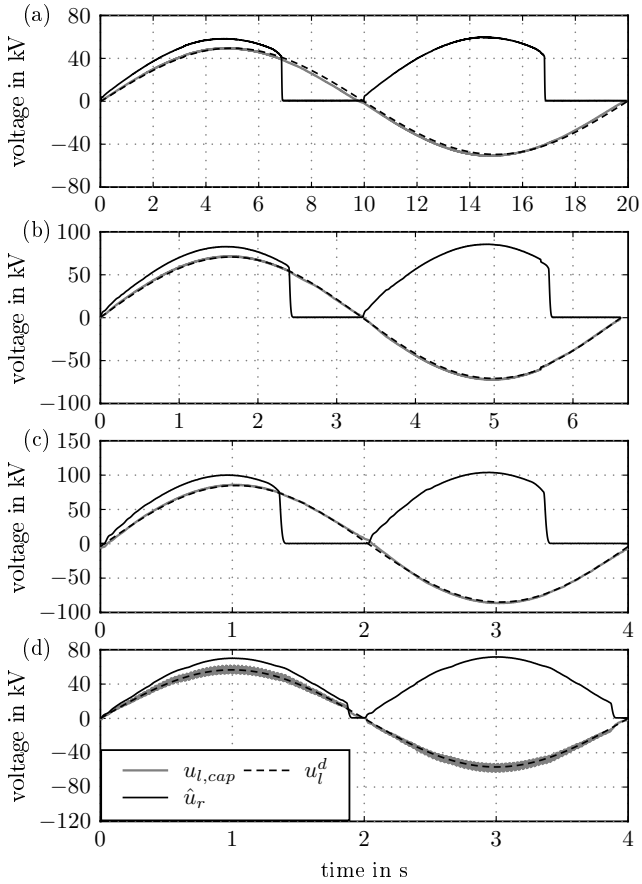

Figure 10: Measurement results: (a) $\hat{U}_{l,0}^d = 35\,\mathrm{kV}$ rms, $C_l = 500\,\mathrm{nF}$, $\hat{C}_l = 504\,\mathrm{nF}$, $\omega_\Delta = 2\pi 0.05\,\mathrm{rad\,s^{-1}}$, (b) $\hat{U}_{l,0}^d = 50\,\mathrm{kV}$ rms, $C_l = 125\,\mathrm{nF}$, $\hat{C}_l = 120\,\mathrm{nF}$, $\omega_\Delta = 2\pi 0.15\,\mathrm{rad\,s^{-1}}$, (c) $\hat{U}_{l,0}^d = 65\,\mathrm{kV}$ rms, $C_l = 125\,\mathrm{nF}$, $\hat{C}_l = 120\,\mathrm{nF}$, $\omega_\Delta = 2\pi 0.25\,\mathrm{rad\,s^{-1}}$, (d) $\hat{U}_{l,0}^d = 35\,\mathrm{kV}$ rms $C_l = 14\,\mathrm{nF}$, $\hat{C}_l = 10\,\mathrm{nF}$, $\omega_\Delta = 2\pi 0.25\,\mathrm{rad\,s^{-1}}$.

Acknowledgment

A main part of the research for this paper has been sponsored by the FFG-Austrian Research Promotion Agency in the BRIDGE-project no. 829582. Further thanks go to Peter Mohaupt and the employees of Mohaupt High Voltage GmbH for providing the DRT prototype and supporting the measurement campaigns.

Appendix A: Model equations

The reduced inductance and resistance matrices $\mathbf{L}_{\Sigma r}$ and $\mathbf{R}_{\Sigma r}$ in (1a) and (5a) are given by

$$\mathbf{L}_{\Sigma r} = \begin{bmatrix} 2L_s + L_r & L_{ps} \\ 2L_{ps} & L_p \end{bmatrix}, \quad \mathbf{R}_{\Sigma r} = \begin{bmatrix} 2R_s + R_r & 0 \\ 0 & R_p \end{bmatrix} \tag{29}$$

with $L_{ps} = k\sqrt{L_p L_s}$ and the capacitance matrix $\mathbf{C}$ in (2) and (7) reads as

$$\mathbf{C} = \begin{bmatrix} C_{dm} + C_r & C_r \\ C_r & C_l + C_r \end{bmatrix}. \tag{30}$$

The current $i_{R_{dm}}$ through the resistive part of the demodulator can be written in the form

$$\begin{aligned} i_{R_{dm}} = \frac{1}{R_{off}} u_{dm} + \left(\frac{1}{R_{dm}^+} - \frac{1}{R_{off}}\right) g^+ \\ + \left(\frac{1}{R_{dm}^-} - \frac{1}{R_{off}}\right) g^-, \end{aligned} \tag{31}$$

with $R_{dm}^+, R_{dm}^- \in [R_{on}, R_{off}]$ and g^+ and g^- defined as

$$g^+ = \begin{cases} u_{dm} & \text{if} \quad u_{dm} \geq 0 \\ 0 & \text{if} \quad u_{dm} < 0 \end{cases}, \qquad g^- = u_{dm} - g^+. \tag{32}$$

The envelope components of the input voltages $\mathbf{U}_\Sigma$ and $\mathbf{U}_\Delta$ in (5a) and (5b) are given by

$$U_{\Sigma,0} = 0 \qquad U_{\Delta,0} = 0 \tag{33a}$$

$$U_{\Sigma,c} = \frac{4}{\pi}\sin(\chi\pi)\, u_p \qquad U_{\Delta,c} = 0 \tag{33b}$$

$$U_{\Sigma,s} = \frac{4}{\pi}(1 - \cos(\chi\pi))\, u_p \qquad U_{\Delta,s} = 0 \tag{33c}$$

The envelope components of $\mathbf{G}^-$ and $\mathbf{G}^+$ are calculated by means of the periodic Fourier transformation Papoulis (1962), with the conditions $u_{dm} \geq 0$ and $u_{dm} < 0$ in (32) described in terms of the envelope components $U_{dm,0}, U_{dm,c}$ and $U_{dm,s}$. In the case $U_{dm,0} > \hat{U}_{dm}$, the resulting envelope components can be written in the form

$$G_0^+ = U_{dm,0}, \quad G_c^+ = U_{dm,c}, \quad G_s^+ = U_{dm,s} \tag{34a}$$

$$G_0^- = 0, \quad G_c^- = 0, \quad G_s^- = 0. \tag{34b}$$

Conversely, for $U_{dm,0} < -\hat{U}_{dm}$, $g^+ = 0$ and $g^- = u_{dm}$, and the envelope components of $\mathbf{G}^-$ and $\mathbf{G}^+$ result in

$$G_0^+ = 0, \quad G_c^+ = 0, \quad G_s^+ = 0 \tag{35a}$$

$$G_0^- = U_{dm,0}, \quad G_c^- = U_{dm,c}, \quad G_s^- = U_{dm,s}. \tag{35b}$$

In the case $-\hat{U}_{dm} \leq U_{dm,0} \leq \hat{U}_{dm}$, the nonlinear term G_0^+ is given by

$$G_0^+ = \left(1 - \frac{\arccos\left(\frac{U_{dm,0}}{\hat{U}_{dm}}\right)}{\pi}\right) U_{dm,0} + \frac{\sqrt{\hat{U}_{dm}^2 - U_{dm,0}^2}}{\pi} \tag{36}$$

and G_0^- reads as

$$G_0^- = U_{dm,0} - G_0^+. \tag{37}$$

Post-print version of the article: W. Kemmetmüller, S. Eberharter, and A. Kugi, "Controller design and experimental validation of a very low frequency high-voltage test system", *Control Engineering Practice*, vol. 37, pp. 32–42, Apr. 2015. DOI: 10.1016/j.conengprac.2014.12.011

The cosine and sine envelope components G_c^+ and G_s^- result in

$$G_c^+ = \left(1 - \frac{\arccos\left(\frac{U_{dm,0}}{\hat{U}_{dm}}\right)}{\pi} + \frac{\sqrt{\hat{U}_{dm}^2 - U_{dm,0}^2}}{\pi}\frac{U_{dm,0}}{\hat{U}_{dm}^2}\right) U_{dm,c}$$
$$= \Psi(U_{dm,0}, \hat{U}_{dm}) U_{dm,c} \tag{38a}$$

$$G_s^+ = \left(1 - \frac{\arccos\left(\frac{U_{dm,0}}{\hat{U}_{dm}}\right)}{\pi} + \frac{\sqrt{\hat{U}_{dm}^2 - U_{dm,0}^2}}{\pi}\frac{U_{dm,0}}{\hat{U}_{dm}^2}\right) U_{dm,s}$$
$$= \Psi(U_{dm,0}, \hat{U}_{dm}) U_{dm,s}, \tag{38b}$$

and G_c^- and G_s^- are given by

$$G_c^- = U_{dm,c} - G_c^+, \qquad G_s^- = U_{dm,s} - G_s^+. \tag{39}$$

Appendix B: Calculation of the control input χ

Applying the transformation of all cosine and sine components given in (14) to (13a), the quasi-stationary equations of the currents result in

$$0 = -R_p \hat{I}_\Sigma \cos(\phi + \phi_\Sigma) + \hat{U}_\Sigma \cos(\phi) - \left(L_p \hat{I}_\Sigma \sin(\phi + \phi_\Sigma) + 2L_{ps} \hat{I}_r \sin(\phi + \phi_r)\right)\omega_r \tag{40a}$$

$$0 = -R_p \hat{I}_\Sigma \sin(\phi + \phi_\Sigma) + \hat{U}_\Sigma \sin(\phi) + \left(L_p \hat{I}_\Sigma \cos(\phi + \phi_\Sigma) + 2L_{ps} \hat{I}_r \cos(\phi + \phi_r)\right)\omega_r \tag{40b}$$

$$0 = -(2R_s + R_r)\hat{I}_r \cos(\phi + \phi_r) + \hat{U}_l \cos(\phi + \phi_l) + \hat{U}_{dm} \cos(\phi + \phi_{dm}) - (L_{ps} \hat{I}_\Sigma \sin(\phi + \phi_\Sigma) + (2L_s + L_r)\hat{I}_r \sin(\phi + \phi_r))\omega_r \tag{40c}$$

$$0 = -(2R_s + R_r)\hat{I}_r \sin(\phi + \phi_r) + \hat{U}_l \sin(\phi + \phi_l) + \hat{U}_{dm} \sin(\phi + \phi_{dm}) + (L_{ps} \hat{I}_\Sigma \sin(\phi + \phi_\Sigma) + (2L_s + L_r)\hat{I}_r \cos(\phi + \phi_r))\omega_r. \tag{40d}$$

Using (14) in (13b) gives

$$0 = -\hat{I}_r \cos(\phi + \phi_r) - \Psi \hat{U}_{dm} \cos(\phi + \phi_{dm}) - ((C_{dm} + C_r)\hat{U}_{dm} \sin(\phi + \phi_{dm}) + C_r \hat{U}_l \sin(\phi + \phi_l))\omega_r \tag{41a}$$

$$0 = -\hat{I}_r \sin(\phi + \phi_r) - \Psi \hat{U}_{dm} \sin(\phi + \phi_{dm}) + ((C_{dm} + C_r)\hat{U}_{dm} \cos(\phi + \phi_{dm}) + C_r \hat{U}_l \cos(\phi + \phi_l))\omega_r \tag{41b}$$

$$0 = -\hat{I}_r \cos(\phi + \phi_r) - \frac{\hat{U}_l \cos(\phi + \phi_l)}{R_l} - (C_r \hat{U}_{dm} \sin(\phi + \phi_{dm}) + (\hat{C}_l + C_r)\hat{U}_l \sin(\phi + \phi_l))\omega_r \tag{41c}$$

$$0 = -\hat{I}_r \sin(\phi + \phi_r) - \frac{\hat{U}_l \sin(\phi + \phi_l)}{R_l} - (C_r \hat{U}_{dm} \cos(\phi + \phi_{dm}) + (\hat{C}_l + C_r)\hat{U}_l \cos(\phi + \phi_l))\omega_r. \tag{41d}$$

By eliminating $\hat{I}_r$ in (41) and substituting the demodulator angle ϕ_{dm} with $\phi_{dm} = \phi_l + \Delta\phi_{dm,l}$, the amplitude $\hat{U}_l$ of the output voltage and the differential angle $\Delta\phi_{dm,l}$ can be calculated

$$\hat{U}_l = \left(\omega_r C_{dm} \sin(\Delta\phi_{dm,l}) + \Psi \cos(\Delta\phi_{dm,l})\right)\hat{U}_{dm} R_l \tag{42a}$$

$$\Delta\phi_{dm,l} = \arctan\left(\frac{\omega_r\left(C_{dm} - R_l \hat{C}_l \Psi\right)}{\Psi + \omega_r^2 R_l \hat{C}_l C_{dm}}\right). \tag{42b}$$

$\hat{I}_r$ and $\Delta\phi_{r,l}$ are calculated using (41c) and (41d) with the angles ϕ_{dm} and ϕ_r replaced by $\phi_{dm} = \phi_l + \Delta\phi_{dm,l}$ and $\phi_r = \phi_l + \Delta\phi_{r,l}$. The results are given by

$$\hat{I}_r = -\frac{\omega_r C_r \hat{U}_{dm} \sin(\Delta\phi_{dm,l}) R_l + \hat{U}_l}{\cos(\Delta\phi_{r,l}) R_l} \tag{43a}$$

$$\Delta\phi_{r,l} = -\arctan\left(\frac{\omega_r R_l(\hat{U}_l \hat{C}_l + C_r \hat{U}_{dm} \cos(\Delta\phi_{dm,l}) + \hat{U}_l C_r}{\omega_r C_r \hat{U}_{dm} \sin(\Delta\phi_{dm,l}) R_l + \hat{U}_l}\right). \tag{43b}$$

By the use of (40c) and (40d) with the angles ϕ_{dm}, ϕ_r and ϕ_Σ substituted by ϕ_l and the differential angles $\Delta\phi_{dm,l}$, $\Delta\phi_{r,l}$ and $\Delta\phi_{\Sigma,l}$, the amplitude $\hat{I}_\Sigma$ of the input current and the differential angle $\Delta\phi_{\Sigma,l}$ yield (44a)-(44b). Finally, (40a) and (40b) are used to calculated the remaining unknowns $\hat{U}_\Sigma$ and ϕ_l, which are given in (45a)-(45b).

References

Baur Prüf- und Messtechnik GmbH (2006). Verfahren zur Erzeugung einer Prüfspannung für die Prüfung elektrischer Betriebsmittel sowie Schaltungsanordnung zur Ausführung des Verfahrens. German Patent DE 195 13 441 B4.

Caliskan, V., Verghese, G., and Stankovic, A. (1996). Multifrequency averaging of dc/dc converters. In *Proc. IEEE workshop on computers in power electronics*, 113–119. Portland, USA.

Chao, Z., Fröhleke, N., and Böcker, J. (2009). Control design for a very low-frequency high-voltage test system. In *Proc. of the 13th European Conference on Power Electronics and Applications*, 1 – 10. Barcelona, Spain.

Chao, Z., Hu, M., Fröhleke, N., and Böcker, J. (2010). Modeling and control design for a very low-frequency high-voltage test system. *IEEE Transactions on Power Electronics*, 25(4), 1068–1077.

Coors, P. and Schierig, S. (2008). Hv ac testing of super-long cables. In *Proc. of the IEEE Int. Symposium on Electrical Insulation*, 636–640. Vancouver, Canada.

Eberharter, S., Kemmetmüller, W., and Kugi, A. (2014). Mathematical Modeling and Analysis of a Very Low Frequency HV Test System. *IEEE Transactions on Power Electronics*, 29(11), 5784 – 5794.

Egretzberger, M. and Kugi, A. (2010). A dynamical envelope model for vibratory gyroscopes. *Microsyst. Technol.*, 16, 777–786.

IEEE Power Engineering Society (2004). *IEEE Guide for Field Testing of Shielded Power Cable Systems Using Very Low Frequency (VLF)*. IEEE Std. 400.2.

J. Hernandez-mejia, R. Harley, N. Hampton, R. Hartlein (2009). Characterization of Ageing for MV Power Cables Using Low Frequency Tan delta Diagnostic Measurements . *IEEE Transactions on Dielectrics and Electrical Insulation*, 16(3), 862–870.

J. Perkel, Y. Del Valle, R.N. Hampton, J.C. Hernandez-mejia, J. Densley (2013). Interpretation of dielectric loss data on service aged polyethylene based power cable systems using VLF test methods. *IEEE Transactions on Dielectrics and Electrical Insulation*, 20(5), 1699–1711.

Post-print version of the article: W. Kemmetmüller, S. Eberharter, and A. Kugi, "Controller design and experimental validation of a very low frequency high-voltage test system", *Control Engineering Practice*, vol. 37, pp. 32–42, Apr. 2015. DOI: 10.1016/j.conengprac.2014.12.011
The content of this post-print version is identical to the published paper but without the publisher's final layout or copy editing.

$$\hat{I}_\Sigma = -\frac{-\hat{U}_l + \omega_r \hat{I}_r L_r \sin(\Delta\phi_{r,l}) + 2\omega_r \hat{I}_r L_s \sin(\Delta\phi_{r,l}) + \hat{I}_r R_r \cos(\Delta\phi_{r,l}) + 2\hat{I}_r R_s \cos(\Delta\phi_{r,l}) - \hat{U}_{dm} \cos(\Delta\phi_{dm,l})}{\omega_r L_{ps} \sin(\Delta\phi_{\Sigma,l})} \tag{44a}$$

$$\Delta\phi_{\Sigma,l} = \operatorname{atan}\left(\frac{-\hat{U}_l + \omega_r \hat{I}_r L_r \sin(\Delta\phi_{r,l}) + 2\omega_r \hat{I}_r L_s \sin(\Delta\phi_{r,l}) + \hat{I}_r R_r \cos(\Delta\phi_{r,l}) + 2\hat{I}_r R_s \cos(\Delta\phi_{r,l}) - \hat{U}_{dm} \cos(\Delta\phi_{dm,l})}{\omega_r \hat{I}_r L_r \cos(\Delta\phi_{r,l}) + 2\omega_r \hat{I}_r L_s \cos(\Delta\phi_{r,l}) + \hat{U}_{dm} \sin(\Delta\phi_{dm,l}) - \hat{I}_r R_r \sin(\Delta\phi_{r,l}) - 2\hat{I}_r R_s \sin(\Delta\phi_{r,l})}\right) \tag{44b}$$

$$\hat{U}_\Sigma = R_p \hat{I}_\Sigma \cos(\phi_l + \Delta\phi_{\Sigma,l}) + \omega_r L_p \hat{I}_\Sigma \sin(\phi_l + \Delta\phi_{\Sigma,l}) + 2\omega_r L_{ps} \hat{I}_r \sin(\phi_l + \Delta\phi_{r,l}) \tag{45a}$$

$$\phi_l = -\Delta\phi_{r,l} - \operatorname{atan}\left(\frac{2\omega_r L_{ps} \hat{I}_r + \omega_r L_p \hat{I}_\Sigma \cos(\Delta\phi_{r,l} - \Delta\phi_{\Sigma,l}) + R_p \hat{I}_\Sigma \sin(\Delta\phi_{r,l} - \Delta\phi_{\Sigma,l})}{\hat{I}_\Sigma(\omega_r L_p \sin(\Delta\phi_{r,l} - \Delta\phi_{\Sigma,l}) - R_p \cos(\Delta\phi_{r,l} - \Delta\phi_{\Sigma,l})}\right) \tag{45b}$$

Kemmetmüller, W., Eberharter, S., and Kugi, A. (2014). Quasi optimal feedforward control of a very low frequency high-voltage test system. In *Proc. of the 19th IFAC World Congress*. Cape Town, South Africa.

Krüger, M., Feurstein, R., and Filz, A. (1990). New very low frequency methods for testing extruded cables. In *Proc. of the IEEE Int. Symposium on Electrical Insulation*, 286–289. Toronto, Canada.

Mohaupt, P. and Bergmann, A. (2010). A new concept for test equipment for testing large hv and uhv cables on-site. *e&i Elektrotechnik und Informationstechnik*, 127(12), 350–353.

Muhr, M., Sumereder, C., and Woschitz, R. (2001). The use of the 0,1 hz cable testing method as substitution to 50 hz measurement and the application for pd measuring and cable fault location. In *Proc. of the 12th Int. Symposium on High Voltage Engineering*. Bangalore, India.

Neumann Elektrotechnik GmbH (2004). Prüfgerät zur Spannungsprüfung von Kabeln und Kabelgarnituren mit VLF Spannung. German Patent DE 103 33 241 B3.

Papoulis, A. (1962). *The Fourier Integral and its Applications*. McGraw-Hill, 1 edition.

Pietsch, R. and Hausschild, W. (2005). Hv on-site testing with partial discharge measurement. In *Brochure of the CIGRE Working Group D1.33.05*.

Putter, H., Götz, D., Petzold, F., and Oetjen, H. (2012). The evolution of vlf testing technologies over the past two decades. In *Proc. of the IEEE Transmission and Distribution Conference and Exposition*, 1–4. Orlando, Florida.

R. Reid (1999). High voltage VLF test equipment with sinusoidal waveform. In *Proc. of the Transmission and Distribution Conference*, 8–12. New Orleans, Louisiana.

Sanders, J.A. and Verhulst, F. (1985). *Averaging Methods in Nonlinear Dynamical Systems*. Springer, New York.

Seesanga, S., Kongnun, W., Sangswang, A., and Chotigo, S. (2008). A new type of the vlf high voltage generator. In *Proc. of the IEEE Int. Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology*, 929 – 932. Krabi, Thailand.

Stanley G. Peschel (2001). Very Low Frequency High Voltage Sinusoidal Electrical Testing Method, Systems and Apparatus. U.S. Patent US 6,169,406 B1.

Post-print version of the article: W. Kemmetmüller, S. Eberharter, and A. Kugi, "Controller design and experimental validation of a very low frequency high-voltage test system", *Control Engineering Practice*, vol. 37, pp. 32–42, Apr. 2015. DOI: 10.1016/j.conengprac.2014.12.011
The content of this post-print version is identical to the published paper but without the publisher's final layout or copy editing.